DECLARATION

I, the undersigned, of 6-1-201, Futamicho, Nishinomiya-shi, Hyogo, Japan, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. **2000-365276**

that was filed in Japanese.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

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[Name of the Document] Specification

[Title of the Invention] Ferroelectric memory

[Claims]

[Claim 1] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

plate lines run in the word line direction above the ferroelectric capacitors of the memory cells adjacent to each other in the word line direction among the plurality of memory cells;

bit line contacts, each connecting a bit line and an active region of the transistor, are placed in regions between the plate lines adjacent to each other in the bit line direction and between the ferroelectric capacitors adjacent to each other in the word line direction;

cut portions are formed at positions of the plate lines near the bit line contacts; and

the active regions of the transistors of the plurality of memory cells extend so as to intersect with the word line direction and the bit line direction.

[Claim 2] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction;

a word line is provided in common for the transistors of the set of memory cells;

a plate line is provided in common for the ferroelectric capacitors of the set of memory cells; and

bit line contacts, each connecting a bit line and an active region of the transistor,

are placed between the plate lines adjacent to each other in the bit line direction.

[Claim 3] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction;

a word line is provided in common for the transistors of the set of memory cells;

plate lines are each provided for the ferroelectric capacitor of each memory cell of the set of memory cells; and

bit line contacts, each connecting a bit line and an active region of the transistor, are placed between plate line groups each composed of a plurality of the plate lines corresponding to the set of memory cells.

[Claim 4] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction;

a plate line is provided in common for the ferroelectric capacitors of the set of memory cells; and

bit line contacts, each connecting a bit line and an active region of the transistor, are placed on both sides of the plate line in the bit line direction.

[Claim 5] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric

memory characterized in that:

active regions of the transistors of the plurality of memory cells extend between the ferroelectric capacitors in the bit line direction; and

word lines each comprise: gate electrode portions, each having a relatively large width, which are formed above portions of the active regions extending between the ferroelectric capacitors in the bit line direction; and interconnection portions of the ferroelectric capacitors, each having a relatively small width and formed to extend in the bit line direction.

[Claim 6] The ferroelectric memory according to Claim 5, characterized in that the active regions each have a bent shape.

[Claim 7] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

among a plurality of the ferroelectric capacitors included in the plurality of memory cells, the ferroelectric capacitors adjacent to each other in the bit line direction with a bit line contact located therebetween are placed so as not to be offset from each other in the word line direction, while the ferroelectric capacitors adjacent to each other in the bit line direction without a bit line contact located therebetween are placed so as to be offset from each other in the word line direction;

active regions of the transistors of the plurality of memory cells extend in the bit line direction between the ferroelectric capacitors adjacent to each other in the word line direction; and

word lines each comprise: gate electrode portions, each having a relatively large width, which are formed above the active regions; and interconnection portions of the

ferroelectric capacitors, each having a relatively small width and formed to extend in the bit line direction.

[Claim 8] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

the ferroelectric capacitors of a pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction;

a plate line is provided in common for the ferroelectric capacitors of the pair of memory cells; and

a word line is provided in common for the transistors of the pair of memory cells and formed between the ferroelectric capacitors of the pair of memory cells.

[Claim 9] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, the ferroelectric memory characterized in that:

the ferroelectric capacitors of each pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction;

an active region of the transistor of one memory cell of each said pair of memory cells extends between the ferroelectric capacitors of the other memory cells of the pairs of memory cells in the bit line direction so as to intersect with a plate line for the other memory cells;

a first word line is provided for the transistor of said one memory cell, while a second word line is provided for the transistor of the other memory cell; and

the second word line is formed to have a small width at its portion intersecting with

the active region of the transistor of said one memory cell to a degree that does not put the active region into an OFF state.

[Claim 10] A ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix,

wherein bit lines are composed of active regions running in the bit line direction between the ferroelectric capacitors of a pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells, and are formed integrally with active regions of the transistors of the plurality of memory cells, and

word lines each comprise: interconnection portions, each having a small width that does not put the bit lines into an OFF state, which are formed above the bit lines; and gate electrode portions, each having a width larger than that of each interconnection portion, which are formed above the active regions of the transistors.

[Detailed Description of the Invention]

[Technical Field to which the Invention Belongs]

The present invention relates to a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix.

[Prior Art]

FIG. **25** shows a circuit configuration of a ferroelectric memory according to first and second conventional examples and embodiments of the present invention. As shown in FIG. **25**, a ferroelectric memory cell is of a one-transistor one-capacitor type having one transistor and one ferroelectric capacitor. A gate electrode of the transistor included in the ferroelectric memory cell is connected to a word line, and a drain electrode of the transistor is connected to a bit line. Further, one electrode of the capacitor included in the ferroelectric memory cell is connected to a plate line, and the other electrode of the

capacitor is connected to a source electrode of the transistor. Thus, the ferroelectric memory cell is controlled by respective signals applied to the plate line, the word line and the bit line.

(First conventional example)

Hereinafter, a ferroelectric memory according to the first conventional example will be described with reference to FIGS. **26**, **27** and **28**.

FIGS. **26** and **27** show a layout of a ferroelectric memory cell array according to the first conventional example, and FIG. **28** shows a cross-sectional structure taken along the line **D-D** of FIGS. **26** and **27**. Note that FIG. **27** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **26**.

Referring to FIGS. **26**, **27** and **28**, the reference characters **11a**, **11b**, **11c** and **11d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **12a**, **12b**, **12c** and **12d** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **13a**, **13b**, **13c** and **13d** denote bit lines made of aluminum interconnections, the reference characters **14a**, **14b**, **14c** and **14d** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **18** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **19** denotes a transistor included in the ferroelectric memory cell **18**. Further, the reference character **15** denotes storage node contacts for connecting the storage nodes **14a**, **14b**, **14c** and **14d** and active regions **16** of the transistors **19**, and the reference character **17** denotes bit line contacts for connecting the bit lines **13a**, **13b**, **13c** and **13d** and the active regions **16** of the transistors **19**.

Referring to FIG. **26**, the reference character **a1** denotes the first inter-plate-line distance between the adjacent plate lines **11a** and **11b** with the bit line contacts **17** located

therebetween, **b1** denotes the line width of the plate lines **11a** and **11b** including the storage nodes **14a**, and **c1** denotes the second inter-plate-line distance between the adjacent plate lines **11b** and **11c** without the bit line contacts **17** located therebetween.

As shown in FIG. **26**, the storage node contact **15** and the bit line contact **17** are placed at the shortest distance from each other via the active region **16**.

(Second conventional example)

Hereinafter, a ferroelectric memory according to the second conventional example will be described with reference to FIGS. **29**, **30** and **31**.

FIGS. **29** and **30** show a layout of a ferroelectric memory cell array according to the second conventional example, and FIG. **31** shows a cross-sectional structure taken along the line **E-E** of FIGS. **29** and **30**. Note that FIG. **30** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **29**.

Referring to FIGS. **29**, **30** and **31**, the reference characters **21a**, **21b**, **21c** and **21d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **22a**, **22b**, **22c** and **22d** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **23a**, **23b**, **23c** and **23d** denote bit lines made of aluminum interconnections, the reference characters **24a**, **24b**, **24c** and **24d** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **28** denotes a one-bit ferroelectric memory cell composed of one transistor and one capacitor, and the reference character **29** denotes the transistor included in the ferroelectric memory cell **28**. Further, the reference character **25** denotes storage node contacts for connecting the storage nodes **24a**, **24b**, **24c** and **24d** and active regions **26** of the transistors **29**, and the reference character **27** denotes bit line contacts for connecting the bit lines **23a**, **23b**, **23c** and **23d** and the active regions **26** of the transistors **29**.

Referring to FIG. **29**, the reference character **a2** denotes the first inter-plate-line distance between the adjacent plate lines **21a** and **21b** with the bit line contacts **27** located therebetween, **b1** denotes the line width of the plate lines **21a** and **21b** including the storage nodes **24a**, **c1** denotes the second inter-plate-line distance between the adjacent plate lines **21b** and **21c** without the bit line contacts **27** located therebetween, the reference character **d** denotes the distance between one side edge of the word line **22a** and the center of the bit line contact **27**, **e** denotes the line width of the word line **22a**, and **f** denotes the distance between the other side edge of the word line **22a** and the center of the storage node contact **25**. Note that the first inter-plate-line distance **a2** in the second conventional example is not the shortest distance obtainable by machining the plate lines **21a** and **21b**.

Actually, the distance between the storage node contact **25** and the bit line contact **27** is set to be the shortest via the active region **26**, which is the sum of the line width **e** of the word line **22a**, the distance **d** between one side edge of the word line **22a** and the center of the bit line contact **27**, and the distance **f** between the other side edge of the word line **22a** and the center of the storage node contact **25**.

[Problems that the Invention is to solve]

(Problems of the first conventional example)

In the first conventional example, the length L11 of the ferroelectric memory cell **18** in the bit line direction satisfies $L11 = a1/2 + b1 + c1/2$.

Therefore, the area S11 of the ferroelectric memory cell **18** is represented by

$$S11 = L11 \times W11 = (a1/2 + b1 + c1/2) \times W11$$

wherein W11 is the length of the ferroelectric memory cell **18** in the word line direction.

In general, a predetermined space is required between the edge of the plate line **11a**, **11b**, **11c** or **11d** on the side of the bit line contacts and the bit line contacts **17** in order to prevent a short circuit therebetween. For this reason, the first inter-plate-line distance **a1**

between the adjacent plate lines **11a** and **11b** with the bit line contacts **17** located therebetween is greater than the second inter-plate-line distance **c1** between the adjacent plate lines **11b** and **11c** without the bit line contacts **17** located therebetween, and therefore, the relationship $a1 > c1$ holds true.

Therefore, in the first conventional example, there arises the problem that the area S11 of the ferroelectric memory cell **18** increases compared with the case in which all the inter-plate-line distances are equal to the second inter-plate-line distance **c1**, that is, $a1 = c1$.

In addition, in the first conventional example, in order to drive the plate line **11a** for read/write of data from/in the ferroelectric memory cell **18**, all of the bit lines **13a, 13b, 13c** and **13d** connected to the plate line **11a** via the word line **12a** are used simultaneously. In this occasion, since the bit lines **13a, 13b, 13c** and **13d** are adjacent to each other, noise is generated due to the capacitance existing between the bit lines, resulting in the problem that a malfunction might easily be caused.

(Problems of the second conventional example)

In the second conventional example, the length L12 of the ferroelectric memory cell **28** in the bit line direction satisfies $L12 = d + e + f + b1/2 + c1/2$.

Since the minimum value of the first inter-plate-line distance **a2** between the adjacent plate lines **21a** and **21b** with the bit line contacts **27** located therebetween is equal to the first inter-plate-line distance **a1** in the first conventional example, the following relationship is satisfied.

$$d + e + f = a2/2 + b1/2 > a1/2 + b1/2$$

From this relationship and the relationship $a1 > c1$ described in the first conventional example, the following relationship is satisfied.

$$d + e + f = a2/2 + b1/2 > c1/2 + b1/2.$$

As a recent tendency, the operating voltage has been increasingly made lower with achievement of finer semiconductor devices; however, ferroelectric capacitors fail to operate sufficiently with a low voltage. Therefore, a voltage higher than the operating voltage for the surrounding circuits must be applied to the ferroelectric capacitors; thus, as transistors included in ferroelectric memory cells, it is necessary to use transistors each having a larger gate length and operating with a higher voltage, compared with transistors located in the surrounding circuits.

However, in the second conventional example, if the gate length of the transistor **29** (= the line width **e** of the word line **22a**) is made large, there arises the problem that the area of the ferroelectric memory cell **28** and thus the area of the ferroelectric memory cell array increase.

In view of the above, a first object of the present invention is to reduce the area of each ferroelectric memory cell, and the second object is to prevent the area of each ferroelectric memory cell from increasing even when the gate length of each transistor is made large.

[Means for Solving the Problems]

To attain the first object, the first ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein plate lines run in the word line direction above the ferroelectric capacitors of the memory cells adjacent to each other in the word line direction among the plurality of memory cells, bit line contacts each connecting a bit line and an active region of the transistor are placed in regions between the plate lines adjacent to each other in the bit line direction and between the ferroelectric capacitors adjacent to each other in the word line direction, cut portions are formed at positions of the plate lines near the bit line contacts, and the active regions of the

transistors of the plurality of memory cells extend so as to intersect with the word line direction and the bit line direction.

In the first ferroelectric memory, cut portions are formed at positions of the plate lines near the bit line contacts, and the active regions of the transistors extend so as to intersect with the word line direction and the bit line direction. Therefore, since the length of each memory cell in the bit line direction can be made small, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the first conventional example.

To attain the first object, the second ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction, a plate line is provided in common for the ferroelectric capacitors of the set of memory cells, and bit line contacts each connecting a bit line and an active region of the transistor are placed between the plate lines adjacent to each other in the bit line direction.

In the second ferroelectric memory, the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction. Therefore, the length of each memory cell in the word line direction is greatly reduced compared with the first conventional example. In addition, a plate line is provided in common for the ferroelectric capacitors of the set of memory cells, and bit line contacts are placed between the plate lines. Therefore, the length of each memory cell in the bit line direction increases only by a rate smaller than the reciprocal of the rate of reduction of the length of each memory cell in the word line direction, compared with the first conventional example. Accordingly, the area of each

memory cell and thus the area of the memory cell array can be reduced compared with the first conventional example.

To attain the first object, the third ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction, a word line is provided in common for the transistors of the set of memory cells, plate lines are each provided for the ferroelectric capacitor of each memory cell of the set of memory cells, and bit line contacts each connecting a bit line and an active region of the transistor are placed between plate line groups each composed of a plurality of the plate lines corresponding to the set of memory cells.

In the third ferroelectric memory, the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction. Therefore, the length of each memory cell in the word line direction is greatly reduced compared with the first conventional example. In addition, bit line contacts are placed between plate line groups each composed of a plurality of the plate lines corresponding to the set of memory cells. Therefore, the length of each memory cell in the bit line direction increases only by a rate smaller than the reciprocal of the rate of reduction of the length of each memory cell in the word line direction, compared with the first conventional example. Accordingly, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the first conventional example.

In the third ferroelectric memory, plate lines are each provided for the ferroelectric capacitor of each memory cell of the set of memory cells. Therefore, although the length

of each memory cell in the bit line direction becomes large compared with the second ferroelectric memory, the bit lines for sending signals to the ferroelectric capacitors of the set of memory cells do not share the same plate line. This prevents generation of noise due to the capacitance existing between the bit lines, which has been described in (Problems of the first conventional example), and thus occurrence of a malfunction due to noise can be prevented.

To attain the first object, the fourth ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction, a plate line is provided in common for the ferroelectric capacitors of the set of memory cells, and bit line contacts each connecting a bit line and an active region of the transistor are placed on both sides of the plate line in the bit line direction.

In the fourth ferroelectric memory, the ferroelectric capacitors of a set of memory cells adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction. Therefore, the length of each memory cell in the word line direction is greatly reduced compared with the first conventional example. In addition, a plate line is provided in common for the ferroelectric capacitors of the set of memory cells, and bit line contacts are placed on both sides of the plate line in the bit line direction. Therefore, the length of each memory cell in the bit line direction increases only by a rate smaller than the reciprocal of the rate of reduction of the length of each memory cell in the word line direction, compared with the first conventional example. Accordingly, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the first conventional example.

To attain the second object, the fifth ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein active regions of the transistors of the plurality of memory cells extend between the ferroelectric capacitors in the bit line direction, and word lines each include: gate electrode portions, each having a relatively large width, which are formed above portions of the active regions extending between the ferroelectric capacitors in the bit line direction; and interconnection portions of the ferroelectric capacitors, each having a relatively small width and formed to extend in the bit line direction.

In the fifth ferroelectric memory, word lines each include: gate electrode portions, each having a relatively large width, which are formed above portions of the active regions extending between the ferroelectric capacitors in the bit line direction; and interconnection portions of the ferroelectric capacitors, each having a relatively small width and formed to extend in the bit line direction. Therefore, it is possible to form the word lines so that both the gate electrode portions and the interconnection portions of the word lines do not protrude from the regions of the plate lines running in the word line direction even when the gate length of each transistor is set equal to the gate length of each transistor in the second conventional example. Accordingly, since the length of each memory cell in the bit line direction can be made small, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the second conventional example.

To attain the second object, the sixth ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein among a plurality of the ferroelectric capacitors included in the plurality of memory cells, the ferroelectric capacitors adjacent to each other in the bit line direction with a bit line contact located

therebetween are placed so as not to be offset from each other in the word line direction, while the ferroelectric capacitors adjacent to each other in the bit line direction without a bit line contact located therebetween are placed so as to be offset from each other in the word line direction, active regions of the transistors of the plurality of memory cells extend in the bit line direction between the ferroelectric capacitors adjacent to each other in the word line direction, and word lines each include: gate electrode portions, each having a relatively large width, which are formed above the active regions; and interconnection portions of the ferroelectric capacitors, each having a relatively small width and formed to extend in the bit line direction.

In the sixth ferroelectric memory, word lines each include: gate electrode portions, each having a relatively large width, which are formed above the active regions; and interconnection portions of the ferroelectric capacitors, each having a relatively small width and formed to extend in the bit line direction. Therefore, it is possible to form the word lines so that both the gate electrode portions and the interconnection portions of the word lines do not protrude from the regions of the plate lines running in the word line direction even when the gate length of each transistor is set equal to the gate length of each transistor in the second conventional example. Accordingly, since the length of each memory cell in the bit line direction can be made small, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the second conventional example.

To attain the second object, the seventh ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein the ferroelectric capacitors of a pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other

in the bit line direction, a plate line is provided in common for the ferroelectric capacitors of the pair of memory cells, and a word line is provided in common for the transistors of the pair of memory cells and formed between the ferroelectric capacitors of the pair of memory cells.

In the seventh ferroelectric memory, a plate line and a word line are provided in common for the ferroelectric capacitors of the pair of memory cells, and the word line is formed between the ferroelectric capacitors of the pair of memory cells. Therefore, since the length of each memory cell in the bit line direction can be made small, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the second conventional example, even when the gate length of each transistor is set equal to the gate length of each transistor in the second conventional example.

In the seventh ferroelectric memory, the line width of the word line is preferably set almost equal to or smaller than the distance between the ferroelectric capacitors of the pair of memory cells.

In that case, the length of each memory cell in the bit line direction can be made further small, and therefore, the area of each memory cell and thus the area of the memory cell array can be further reduced.

To attain the second object, the eighth ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein the ferroelectric capacitors of each pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells are placed so as to be offset from each other in the bit line direction, an active region of the transistor of one memory cell of each said pair of memory cells extends between the ferroelectric capacitors of the other memory cells of the pairs of memory cells in the bit line direction so as to intersect with a plate line

for the other ferroelectric memory cells, a first word line is provided for the transistor of said one memory cell, while a second word line is provided for the transistor of the other memory cell, and the second word line is formed to have a small width at its portion intersecting with the active region of the transistor of said one memory cell to a degree that does not put the active region into an OFF state.

In the eighth ferroelectric memory, the second word line is formed to have a small width at its portion intersecting with the active region of the transistor of said one memory cell to a degree that does not put the active region into an OFF state. Therefore, since the length of each memory cell in the bit line direction can be made small, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the second conventional example, even when the gate length of each transistor is set equal to the gate length of each transistor in the second conventional example.

To attain the second object, the ninth ferroelectric memory according to the present invention is a ferroelectric memory in which a plurality of memory cells each having a transistor and a ferroelectric capacitor are arranged in a matrix, wherein bit lines are composed of active regions running in the bit line direction between the ferroelectric capacitors of a pair of memory cells adjacent to each other in the word line direction among the plurality of memory cells, and are formed integrally with active regions of the transistors of the plurality of memory cells, and word lines each include: interconnection portions, each having a small width that does not put the bit line into an OFF state, which are formed above the bit lines; and gate electrode portions, each having a width larger than that of each interconnection portion, which are formed above the active regions of the transistors.

In the ninth ferroelectric memory, word lines each include: interconnection portions, each having a small width that does not put the bit line into an OFF state, which

are formed above the bit lines; and gate electrode portions, each having a width larger than that of each interconnection portion, which are formed above the active regions of the transistors. Therefore, since the length of each memory cell in the bit line direction can be made small, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the second conventional example, even when the gate length of each transistor is set equal to the gate length of each transistor in the second conventional example.

[Embodiments of the Invention]

(First embodiment)

Hereinafter, a ferroelectric memory according to the first embodiment will be described with reference to FIGS. **1**, **2** and **3**.

FIGS. **1** and **2** show a layout of a ferroelectric memory cell array according to the first embodiment, and FIG. **3** shows a cross-sectional structure taken along the line **A-A** of FIGS. **1** and **2**. Note that FIG. **2** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **1**.

Referring to FIGS. **1**, **2** and **3**, the reference characters **101a**, **101b**, **101c** and **101d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **102a**, **102b**, **102c** and **102d** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **103a**, **103b**, **103c** and **103d** denote bit lines made of aluminum interconnections, the reference characters **104a**, **104b**, **104c** and **104d** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **108** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **109** denotes a transistor included in the ferroelectric memory cell **108**. Further, the reference character **105a** denotes a storage node contact for

connecting the storage node **104a** and an active region **106** of the transistor **109**, and the reference character **107** denotes a bit line contact for connecting the bit line **103a** and the active region **106** of the transistor **109**.

Furthermore, referring to FIG. **1**, the reference character **b1** denotes the line width of the plate lines **101a** through **101d** including the storage nodes **104a** through **104d**, **c1** denotes the first inter-plate-line distance between the adjacent plate lines **101b** and **101c** without the bit line contacts **107** located therebetween, and **c2** denotes the second inter-plate-line distance between the adjacent plate lines **101a** and **101b** with the bit line contacts **107** located therebetween.

As shown in FIG. **1**, the plate lines **101a** through **101d** run in the word line direction (lateral direction in FIG. **1**) above the storage nodes **104a** through **104d** of the ferroelectric memory cells **108** adjacent to each other in the word line direction.

The bit lines **103a** through **103d** run in the bit line direction (vertical direction in FIG. **1**) between the storage nodes **104a** through **104d** of the ferroelectric memory cells adjacent to each other in the word line direction.

The bit line contact **107** is placed under the bit line **103a** and between the plate lines (**101a** and **101b**) adjacent to each other in the bit line direction.

Cut portions are formed at positions of the plate line **101a** near the bit line contacts **107**, thus securing a predetermined gap between the side edge of the plate line **101a** and the bit line contacts **107**.

The word line **102a** runs in a zigzag fashion navigating around the storage node contacts **105** and the bit line contacts **107**.

The active region **106** of the transistor **109** is formed into an L shape so as to connect a pair of storage node contacts **105a** and **105b** adjacent to each other in the bit line direction and the bit line contact **107** adjacent to the pair of storage node contacts **105a** and

105b, thus allowing the active region **106** of the transistor **109** to extend so as to intersect with the word line direction and the bit line direction.

In the first embodiment, the second inter-plate-line distance **c2** is set equal to the first inter-plate-line distance **c1**.

Therefore, the length L1 of the ferroelectric memory cell **108** in the bit line direction satisfies $L1 = b1 + c1$.

Besides, in the first conventional example, the length L11 of the ferroelectric memory cell **18** in the bit line direction satisfies $L11 = a1/2 + b1 + c1/2$, and therefore, the difference between the length of the ferroelectric memory cell in the bit line direction in the first conventional example and that of the ferroelectric memory cell in the bit line direction in the first embodiment, i.e., $L11 - L1$, satisfies $L11 - L1 = (a1 - c1)/2$.

Since the relationship $a1 > c1$ holds true as described before, the relationship $L11 > L1$ is established.

Thus, the area of the ferroelectric memory cell **108** in the first embodiment is smaller than the area of the ferroelectric memory cell **18** in the first conventional example.

(Modification of the first embodiment)

FIG. **4** shows a layout of a ferroelectric memory cell array according to a modification of the first embodiment.

In the first embodiment, the active region **106** of the transistor **109** is formed into an L shape so as to connect the pair of storage node contacts **105a** and **105b** adjacent to each other in the bit line direction and the bit line contact **107** adjacent to the pair of storage node contacts **105a** and **105b**. In this modification, however, the active region **106** of the transistor **109** is formed into a straight-line shape so as to connect a pair of storage node contacts **105a** and **105b** adjacent to each other in the bit line direction and the word line direction, i.e., in an oblique direction, and the bit line contact **107** located between the

pair of storage node contacts **105a** and **105b**, thus allowing the active region **106** of the transistor **109** to extend so as to intersect with the word line direction and the bit line direction.

(Second embodiment)

Hereinafter, a ferroelectric memory according to the second embodiment will be described with reference to FIGS. **5** and **6**.

FIGS. **5** and **6** show a layout of a ferroelectric memory cell array according to the second embodiment. Note that FIG. **6** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **5**.

Referring to FIGS. **5** and **6**, the reference characters **201a** and **201b** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **202a** and **202b** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **203a, 203b, 203c, 203d, 203e, 203f, 203g** and **203h** denote bit lines made of aluminum interconnections, the reference characters **204a**, **204b**, **204c**, **204d**, **204e**, **204f**, **204g** and **204h** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **208** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference characters **209a** and **209b** denote transistors included in the ferroelectric memory cell **208**. Further, the reference character **205** denotes storage node contacts for connecting the storage nodes **204a** through **204h** and active regions **206** of the transistors **209a** and **209b**, and the reference character **207** denotes bit line contacts for connecting the bit lines **203a** through **203h** and the active regions **206** of the transistors **209a** and **209b**.

Furthermore, referring to FIG. **5**, the reference character **a1** denotes the distance between the adjacent plate lines **201a** and **201b** with the bit line contacts **207** located

therebetween, **b1** denotes the line width of the plate lines **12a** and **12b** including the storage nodes in the first conventional example, **b2** denotes the line width of the plate lines **201a** and **202b** each including the storage nodes **204a** through **204h** arranged in two lines, and **c1** denotes the distance between each pair of the storage nodes (**204a** and **204b**), (**204c** and **204d**), (**204e** and **204f**) and (**204g** and **204h**) adjacent to each other in the bit line direction.

As shown in FIG. **5**, the storage nodes (**204a** and **204b**), (**204c** and **204d**), (**204e** and **204f**) and (**204g** and **204h**) of the ferroelectric capacitors of the respective pairs of the ferroelectric memory cells **208** adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction.

Note that the length of the ferroelectric memory cell **208** in the word line direction is set at a half of that of the ferroelectric memory cell **18** in the word line direction according to the first conventional example.

The plate lines **201a** and **201b** are each provided in common for the storage nodes **204a** through **204h** of the ferroelectric capacitors of the pairs of the memory cells placed at positions offset from each other in the bit line direction.

The word lines **202a** and **202b** are each provided in common for the transistors **209a** and **209b** corresponding to the storage nodes **204a** through **204h** of the ferroelectric capacitors placed so as to be offset from each other in the bit line direction.

The bit lines **203a** through **203h** run above the respective storage nodes **204a** through **204h**.

The bit line contacts **207** are placed under the respective bit lines **203a** through **203h** and between the plate lines **201a** and **201b** adjacent to each other in the bit line direction.

Actually, the plate lines **201a** and **202b** and the storage nodes **204a** through **204h** are made of the same material, and thus the machinable minimum spacing is the same.

Therefore, the distance **c1** between each pair of the storage nodes (**204a** and **204b**), (**204c** and **204d**), (**204e** and **204f**) and (**204g** and **204h**) adjacent to each other in the bit line direction is equal to the second inter-plate-line distance **c1** in the first conventional example.

In the second embodiment, the line width **b2** of the plate lines **201a** and **202b** including the storage nodes **204a** through **204h** arranged in two lines satisfies the relationship $b2 < 2b1 + c1$.

Therefore, the length L2 of the ferroelectric memory cell **208** in the bit line direction satisfies the relationship:

$$L2 = a1/2 + b2 + c1/2$$
$$< a1/2 + 2b1 + c1 + c1/2.$$

The length of the ferroelectric memory cell **208** in the word line direction according to the second embodiment is a half of the length W11 of the ferroelectric memory cell **18** in the word line direction according to the first conventional example, and thus the area S2 of the ferroelectric memory cell **208** according to the second embodiment satisfies the relationship:

$$S2 = (a1/2 + b2 + c1/2) \times W11/2$$
$$< (a1/2 + 2b1 + c1 + c1/2) \times W11/2$$
$$< (a1/2 + b1 + c1/2) \times W11 - (a1 - c1) \times W11/4.$$

As described before, the area S11 of the ferroelectric memory cell **18** according to the first conventional example satisfies $S11 = (a1/2 + b1 + c1/2) \times W11$, and the value of $(a1 - c1)$ is positive; therefore, the area S2 of the ferroelectric memory cell **208** according to the second embodiment is smaller than the area S11 of the ferroelectric memory cell **18** according to the first conventional example.

(Third embodiment)

Hereinafter, a ferroelectric memory according to the third embodiment will be described with reference to FIGS. **7** and **8**.

FIGS. **7** and **8** show a layout of a ferroelectric memory cell array according to the third embodiment. Note that FIG. **8** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **7**.

Referring to FIGS. **7** and **8**, the reference characters **301a**, **301b**, **301c** and **301d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **302a** and **302b** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **303a**, **303b**, **303c**, **303d**, **303e**, **303f**, **303g** and **303h** denote bit lines made of aluminum interconnections, the reference characters **304a**, **304b**, **304c**, **304d**, **304e**, **304f**, **304g** and **304h** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **308** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference characters **309a** and **309b** denote transistors included in the ferroelectric memory cell **308**. Further, the reference character **305** denotes storage node contacts for connecting the storage nodes **304a** through **304h** and active regions **306** of the transistors **309a** and **309b**, and the reference character **307** denotes bit line contacts for connecting the bit lines **303a** through **303h** and the active regions **306** of the transistors **309a** and **309b**.

Referring to FIG. **7**, the reference character **a1** denotes the first inter-plate-line distance between the plate lines **301b** and **301c** with the bit line contacts **307** located therebetween, **b1** denotes the line width of the plate lines **301a** through **301d** including the storage nodes **304a** through **304h**, and **c1** denotes the second inter-plate-line distance between the plate lines **301a** and **301b** without the bit line contacts **307** located therebetween.

As shown in FIG. **7**, the storage nodes (**304a** and **304b**), (**304c** and **304d**), (**304e** and **304f**) and (**304g** and **304h**) of the ferroelectric capacitors of respective pairs of the ferroelectric memory cells **308** adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction.

Note that the length of the ferroelectric memory cell **308** in the word line direction is set at a half of that of the ferroelectric memory cell **18** in the word line direction according to the first conventional example.

The word lines **302a** and **302b** are each provided in common for the transistors **309a** and **309b** corresponding to the storage nodes **304a** through **304h** of the pairs of the ferroelectric capacitors placed so as to be offset from each other in the bit line direction.

The plate lines **301a** and **301b** are respectively provided for the storage nodes (**304a**, **304c**, **304e** and **304g**) and the storage nodes (**304b**, **304d**, **304f** and **304h**) of the ferroelectric capacitors located on the same lines in the word line direction. That is, two plate lines **301a** and **301b** are provided for each of the word lines **302a** and **302b**.

In the third embodiment, the length L3 of the ferroelectric memory cell **308** in the bit line direction satisfies the relationship $L3 = (a1/2) + 2b1 + c1 + (c1/2)$.

The length of the ferroelectric memory cell **308** in the word line direction according to the third embodiment is a half of the length W11 of the ferroelectric memory cell **18** in the word line direction according to the first conventional example, and thus the area S3 of the ferroelectric memory cell **308** according to the third embodiment satisfies the relationship:

$$S3 = (a1/2 + 2b1 + c1 + c1/2) \times W11/2$$
$$< (a1/2 + b1 + c1/2) \times W11 - (a1 - c1) \times W11/4.$$

As described before, the area S11 of the ferroelectric memory cell **18** according to the first conventional example satisfies $S11 = (a1/2 + b1 + c1/2) \times W11$, and the value of

(a1 – c1) is positive; therefore, the area S3 of the ferroelectric memory cell **308** according to the third embodiment is smaller than the area S11 of the ferroelectric memory cell **18** according to the first conventional example.

Moreover, in the third embodiment, during data read/write from/in the ferroelectric memory cell **308**, only the plate line **301a** is driven, and therefore, the bit lines **303a, 303b, 303c** and **303d**, which are not adjacent to each other, are connected to the plate line **301a** via the word line **302a**. Furthermore, the bit line **303a** and the bit line **303e** adjacent to the bit line **303a**, for example, do not share the same plate line. Therefore, occurrence of a malfunction due to noise is prevented.

(Fourth embodiment)

Hereinafter, a ferroelectric memory according to the fourth embodiment will be described with reference to FIGS. **9** and **10**.

FIGS. **9** and **10** show a layout of a ferroelectric memory cell array according to the fourth embodiment. Note that FIG. **10** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **9**.

Referring to FIGS. **9** and **10**, the reference character **401** denotes a plate line constructed of upper electrodes of ferroelectric capacitors, the reference characters **402a** and **402b** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **403a, 403b**, **403c**, **403d**, **403e, 403f, 403g** and **403h** denote bit lines made of aluminum interconnections, the reference characters **404a, 404b**, **404c**, **404d**, **404e**, **404f**, **404g** and **404h** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **408** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **409** denotes a transistor included in the ferroelectric memory cell **408**. Further, the reference character **405** denotes

storage node contacts for connecting the storage nodes **404a** through **404h** and active regions **406** of the transistors **409**, and the reference character **407** denotes bit line contacts for connecting the bit lines **403a** through **403h** and the active regions **406** of the transistors **409**.

Furthermore, referring to FIG. **9**, the reference character **a1** denotes the distance between the adjacent plate lines **401** with the bit line contacts **407** located therebetween, **b1** denotes the line width of the plate lines **11a** and **11b** including the storage nodes in the first conventional example, **b2** denotes the line width of the plate line **401a**, **402b** including the storage nodes **404a** through **404h** arranged in two lines, and **c1** denotes the distance between each pair of the storage nodes (**404a** and **404b**), (**404c** and **404d**), (**404e** and **404f**) and (**404g** and **404h**) adjacent to each other in the bit line direction.

As shown in FIG. **9**, the storage nodes (**404a** and **404b**), (**404c** and **404d**), (**404e** and **404f**) and (**404g** and **404h**) of the ferroelectric capacitors of respective pairs of the ferroelectric memory cells **408** adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction.

Note that the length of the ferroelectric memory cell **408** in the word line direction is set at a half of that of the ferroelectric memory cell **18** in the word line direction according to the first conventional example.

The plate line **401** is provided in common for the storage nodes **404a** through **404h** of the ferroelectric capacitors of the pairs of the memory cells placed at positions offset from each other in the bit line direction.

The word lines **402a** and **402b** are respectively provided for the storage nodes (**404a**, **404c**, **404e** and **404g**) and the storage nodes (**404b**, **404d**, **404f** and **404h**) of the ferroelectric capacitors located on the same lines in the word line direction. That is, one plate line **401** is provided for the two word lines **402a** and **402b**.

The bit lines **403a** through **403h** run above the respective storage nodes **404a** through **404h**.

The bit line contacts **407** are placed under the bit lines **403a** through **403h** and between the plate lines **401** adjacent to each other in the bit line direction.

Actually, the plate line **401** and the storage nodes **404a** through **404h** are made of the same material, and thus the machinable minimum spacing is the same; therefore, the distance **C1** between each pair of the storage nodes (**404a** and **404b**), (**404c** and **404d**), (**404e** and **404f**) and (**404g** and **404h**) adjacent to each other in the bit line direction is equal to the second inter-plate-line distance **C1** in the first conventional example.

In the fourth embodiment, the line width **b2** of the plate line **401** including the storage nodes **404a** through **404h** arranged in two lines satisfies the relationship $b2 < 2b1 + c1$.

The length L4 of the ferroelectric memory cell **408** in the bit line direction according to the fourth embodiment satisfies the relationship $L4 = a1 + b2 < a1 + 2b1 + c1$.

The length of the ferroelectric memory cell **408** in the word line direction according to the fourth embodiment is a half of the length W11 of the ferroelectric memory cell **18** in the word line direction according to the first conventional example; in addition, as described before, the area S11 of the ferroelectric memory cell **18** according to the first conventional example satisfies $S11 = (a1/2 + b1 + c1/2) \times W11$, and thus the area S4 of the ferroelectric memory cell **408** according to the fourth embodiment satisfies the relationship:

$$
\begin{aligned}
S4 &= (a1 + 2b1) \times W11/2 \\
&< (a1 + 2b1 + c1) \times W11/2 \\
&< (a1/2 + b1 + c1/2) \times W11 = S11.
\end{aligned}
$$

Therefore, the area S4 of the ferroelectric memory cell **408** according to the fourth

embodiment is smaller than the area S11 of the ferroelectric memory cell **18** according to the first conventional example.

(Modification of the fourth embodiment)

FIG. **11** shows a layout of a ferroelectric memory cell array according to a modification of the fourth embodiment.

In this modification, as in the first embodiment, cut portions are formed at positions of the plate line **401** near the bit line contacts **407**, the word lines **402a** and **402b** run in a zigzag fashion navigating around the storage node contacts **405** and the bit line contacts **407**, and the active regions **406** are each formed into an L shape so as to connect a pair of the storage node contacts **405** adjacent to each other in the bit line direction and the bit line contact **407** adjacent to the pair of storage node contacts **405**.

(Fifth embodiment)

Hereinafter, a ferroelectric memory according to the fifth embodiment will be described with reference to FIGS. **12**, **13** and **14**.

FIGS. **12** and **13** show a layout of a ferroelectric memory cell array according to the fourth embodiment, and FIG. **14** shows a cross-sectional structure taken along the line **B-B** of FIGS. **12** and **13**. Note that FIG. **13** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **12**.

Referring to FIGS. **12**, **13** and **14**, the reference characters **501a**, **501b**, **501c** and **501d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **502a**, **502b**, **502c** and **502d** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **503a**, **503b**, **503c** and **503d** denote bit lines made of aluminum interconnections, the reference characters **504a**, **504b**, **504c** and **504d** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the

reference character **508** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **509** denotes a transistor included in the ferroelectric memory cell **508**. Further, the reference character **505** denotes storage node contacts for connecting the storage nodes **504a** through **504d** and active regions **506** of the transistors **509**, and the reference character **507** denotes bit line contacts for connecting the bit lines **503a** through **503d** and the active regions **506** of the transistors **509**.

Furthermore, referring to FIG. **12**, the reference character **a1** denotes the first inter-plate-line distance between the adjacent plate lines **501a** and **501b** with the bit line contacts **507** located therebetween, **b1** denotes the line width of the plate lines **501a** through **501d** each including the storage nodes **504a** through **504d**, and **c1** denotes the second inter-plate-line distance between the adjacent plate lines **501b** and **501c** without the bit line contacts **507** located therebetween.

As shown in FIG. **12**, the plate lines **501a** through **501d** run in the word line direction above the storage nodes **504a** through **504d** of the ferroelectric memory cells adjacent to each other in the word line direction.

The bit lines **503a** through **503d** run between the storage nodes **504a** through **504d** of the ferroelectric memory cells adjacent to each other in the word line direction.

The bit line contacts **507** are placed under the bit lines **503a** through **503d**, and placed between the plate lines (**501a** and **501b**) and between the plate lines (**501c** and **501d**) adjacent to each other in the bit line direction.

The active regions **506** of the transistors **509a** and **509b** extend from a pair of the storage node contacts **505a** and **505b**, located adjacent to each other in the bit line direction, so as to be separated from each other, bend toward the bit line **503a**, and then extend under the bit line **503a**, i.e., in the bit line direction between the storage nodes.

Each of the word lines **502a** through **502d** has: gate electrode portions, each having

a relatively large width, which are formed above portions of the active regions **506** extending between the storage nodes **504a** through **504d** in the bit line direction; and interconnection portions, each having a relatively small width, which are formed near the storage nodes **504a** through **504d**.

Now, in the fifth embodiment, each of the word lines **502a** through **502d** has: gate electrode portions, each having a relatively large width, which are formed above portions of the active regions **506** extending between the storage nodes **504a** through **504d** in the bit line direction; and interconnection portions, each having a relatively small width, which are formed near the storage nodes **504a** through **504d**. Therefore, it is possible to form the word lines **502a** through **502d** so that they do not protrude from the plate lines **501a** through **501d** even when the gate length of the transistor **509** is set equal to that of the transistor **29** in the second conventional example.

The length L5 of the ferroelectric memory cell **508** in the bit line direction according to the fifth embodiment satisfies $L5 = a1/2 + b1 + c1/2$.

On the other hand, the length L12 of the ferroelectric memory cell **28** in the bit line direction according to the second conventional example satisfies $L12 = d + e + f + b1/2 + c1/2$.

Therefore, $L12 - L5 = (d + e + f) - (a1/2 + b1/2)$ holds true.

Now, since the relationship $d + e + f = a2/2 + b1/2 > a1/2 + b1/2$ is established as described in (Problems of the second conventional example), $L12 > L5$ holds true.

Therefore, the area of the ferroelectric memory cell **508** according to the fifth embodiment can be smaller than the area of the ferroelectric memory cell **28** according to the second conventional example.

In that case, the greater the gate length (= e) of the transistor **509**, the greater the difference between the area of the ferroelectric memory cell **508** according to the fifth

embodiment and the area of the ferroelectric memory cell **28** according to the second conventional example.

(Sixth embodiment)

Hereinafter, a ferroelectric memory according to the sixth embodiment will be described with reference to FIGS. **15**, **16** and **17**.

FIGS. **15** through **17** show a layout of a ferroelectric memory cell array according to the sixth embodiment. Note that FIG. **16** shows only plate lines, word lines, bit lines, storage nodes and bit line contacts extracted from the layout shown in FIG. **15**, and FIG. **17** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **15**.

Referring to FIGS. **15** through **17**, the reference characters **601a**, **601b**, **601c** and **601d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **602a**, **602b**, **602c** and **602d** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **603a**, **603b**, **603c** and **603d** denote bit lines made of aluminum interconnections, the reference characters **604a**, **604b**, **604c** and **604d** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **608** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **609** denotes a transistor included in the ferroelectric memory cell **608**. Further, the reference character **605** denotes a storage node contact for connecting the storage node **604a** and an active region **606** of the transistor **609**, and the reference character **607** denotes a bit line contact for connecting the bit line **603a** and the active region **606** of the transistor **609**.

Referring to FIGS. **15** and **16**, the reference character **a1** denotes the first inter-plate-line distance between the adjacent plate lines (**601a** and **601b**) and (**601c** and **601d**)

with the bit line contacts **607** located therebetween, **b1** denotes the line width of the plate lines **601a** through **601d** each including the storage nodes **604a** through **604d**, and **c1** denotes the second inter-plate-line distance between the adjacent plate lines **601b** and **601c** without the bit line contacts **607** located therebetween.

As shown in FIG. **15**, the storage nodes of the ferroelectric capacitors of the ferroelectric memory cells (**608a** and **608b**) adjacent to each other in the bit line direction via the bit line contact **607** (i.e., the storage node **604a** in the first line and the storage node **604e** in the fourth line) are placed so as not to be offset from each other in the word line direction (located so as to be aligned in the bit line direction). On the other hand, the storage nodes of the ferroelectric capacitors of the ferroelectric memory cells (**608a** and **608c**, or **608b** and **608d**) that share the same bit line and are adjacent to each other without the bit line contact **607** located therebetween (i.e., the storage node **604a** in the first line and the storage node **604f** in the second line, or the storage node **604g** in the third line and the storage node **608b** in the fourth line) are placed so as to be offset from each other in the word line direction.

Note that the length of the ferroelectric memory cell **608** in the word line direction is set at a half of that of the ferroelectric memory cell **28** in the word line direction according to the second conventional example.

The bit line **603a** runs in the bit line direction, bends in the word line direction at a position between the ferroelectric memory cells (**608a** and **608c**), which share the same bit line and are adjacent to each other without the bit line contact **607** located therebetween, and then runs in the bit line direction between the storage nodes of the ferroelectric capacitors of the memory cells (**608a** and **608b**) adjacent to each other in the bit line direction via the bit line contact **607** (i.e., between the storage node **604a** in the first line and the storage node **608b** in the fourth line). Thereafter, the bit line **603a** bends in the

word line direction at a position between the storage nodes of the ferroelectric capacitors of the memory cells (**608b** and **608d**), which share the same bit line and are adjacent to each other without the bit line contact **607** located therebetween (i.e., between the storage node **604g** in the third line and the storage node **608b** in the fourth line), and then runs in the bit line direction.

The active region **606** extends between a pair of the storage nodes (i.e., the storage nodes in the first line and in the fourth line) that share the bit line contact **607** and are placed so as not to be offset from each other in the word line direction.

Therefore, the word line **602b** is operated when the plate line **601a** is driven, while the word line **602a** is operated when the plate line **601b** is driven.

Each of the word lines **602a** through **602d** has: gate electrode portions, each having a relatively large width, which are formed above the active regions **606**; and interconnection portions, each having a relatively small width, which are formed near the storage nodes **604a** through **604d**.

In the sixth embodiment, the word line **602b** has: gate electrode portions, each having a relatively large width, which are formed above the active regions **606**; and interconnection portions, each having a relatively small width, which are formed near the storage nodes **604a** through **604d**; therefore, it is possible to set the gate length of the transistor **609** to be equal to that of the transistor **29** in the second conventional example only above the active regions **606**.

The length L6 of the ferroelectric memory cell **608** in the bit line direction according to the sixth embodiment satisfies $L6 = a1 + 2b1 + c1$.

The length of the ferroelectric memory cell **608** in the word line direction according to the sixth embodiment is a half of the length W12 of the ferroelectric memory cell **28** in the word line direction according to the second conventional example, and therefore, the

area S6 of the ferroelectric memory cell **608** according to the sixth embodiment satisfies

$$S6 = (a1 + 2b1 + c1) \times W12/2$$

$$= (a1/2 + b1 + c1/2) \times W12.$$

On the other hand, the area S12 of the ferroelectric memory cell **28** according to the second conventional example satisfies $S12 = (d + e + f + b1/2 + c1/2) \times W12$.

Therefore, $S12 - S6 = \{(d + e + f) - (a1/2 + b1/2)] \times W12$ holds true.

Now, since the relationship $d + e + f = a2/2 + b1/2 > a1/2 + b1/2$ is established as described in (Problems of the second conventional example), $S12 > S6$ holds true.

Thus, the area of the ferroelectric memory cell **608** according to the sixth embodiment can be made smaller than the area of the ferroelectric memory cell **28** according to the second conventional example.

In this case, the greater the gate length (= e) of the transistor **609**, the greater the difference between the area S6 of the ferroelectric memory cell **508** according to the sixth embodiment and the area S12 of the ferroelectric memory cell **28** according to the second conventional example.

(Seventh embodiment)

Hereinafter, a ferroelectric memory according to the seventh embodiment will be described with reference to FIGS. **18** and **19**.

FIGS. **18** and **19** show a layout of a ferroelectric memory cell array according to the seventh embodiment. Note that FIG. **19** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **18**.

Referring to FIGS. **18** and **19**, the reference character **701** denotes a plate line constructed of upper electrodes of ferroelectric capacitors, the reference character **702** denotes a word line made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **703a**, **703b**, **703c**, **703d**, **703e**, **703f**, **703g** and

703h denote bit lines made of aluminum interconnections, the reference characters **704a**, **704b**, **704c**, **704d**, **704e**, **704f**, **704g** and **704h** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **708** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **709** denotes a transistor included in the ferroelectric memory cell **708**. Further, the reference character **705** denotes storage node contacts for connecting the storage nodes **704a** through **704h** and active regions **706** of the transistors **709**, and the reference character **707** denotes bit line contacts for connecting the bit lines **703a** through **703h** and the active regions **706** of the transistors **709**.

Referring to FIG. **18**, the reference character **a1** denotes the distance between the adjacent plate lines **701** with the bit line contacts **707** located therebetween, **b1** denotes the line width of the plate lines **21a** and **21b** including the storage nodes in the second conventional example, **b2** denotes the line width of the plate line **701** including the storage nodes **704a** through **704h** arranged in two lines, and **c1** denotes the distance between the adjacent plate lines **21b** and **21c** without the bit line contacts **27** in the second conventional example located therebetween.

As shown in FIG. **18**, the plate line **701** is provided in common for the storage nodes **704a** through **704h** of the ferroelectric capacitors in two lines (for example, the storage nodes **704a**, **704c**, **704e** and **704g** in the second line, and the storage nodes **704b**, **704d**, **704f** and **704h** in the third line).

Among the storage nodes **704a** through **704h** of the ferroelectric capacitors in two lines which share the plate line **701**, the storage nodes **704a**, **704c**, **704e** and **704g** in one line (for example, in the second line) are placed so as to be offset from the storage nodes **704b**, **704d**, **704f** and **704h** in the other line (for example, in the third line) in the bit line direction.

Note that the length of the ferroelectric memory cell **708** in the word line direction is set at a half of that of the ferroelectric memory cell **28** in the word line direction according to the second conventional example.

The word line **702** is located between the ferroelectric capacitors in two lines which share the plate line **701** (for example, between the storage nodes **704a**, **704c**, **704e** and **704g** in the second line and the storage nodes **704b**, **704d**, **704f** and **704h** in the third line), and is provided in common for the transistors **709** corresponding to the ferroelectric capacitors in the two lines which share the plate line **701**.

The bit lines **703a** through **703h** are provided for the respective ferroelectric capacitors in the two lines which share the plate line **701**, and the bit line contacts **707** are placed under the bit lines **703a** through **703h** and between the plate lines **701**.

Actually, the plate line **701** and the storage nodes **704a** through **704h** are made of the same material, and thus the machinable minimum spacing is the same. Therefore, among the storage nodes **704a** through **704h** of the ferroelectric capacitors in two lines which share the plate line **701**, the distance **C1** between the storage nodes **704a**, **704c**, **704e** and **704g** in one line (for example, in the second line) and the storage nodes **704b**, **704d**, **704f** and **704h** in the other line (for example, in the third line) is equal to the second inter-plate-line distance **C1** in the second conventional example.

Furthermore, the line width of the word line **702**, that is, the gate length of the transistor **709** can be set to be roughly the same as the distance between the storage nodes **704a**, **704c**, **704e** and **704g** in one line (for example, in the second line) and the storage nodes **704b**, **704d**, **704f** and **704h** in the other line (for example, in the third line) among the storage nodes **704a** through **704h** of the ferroelectric capacitors in two lines which share the plate line **701**. Therefore, the area of the ferroelectric memory cell **708** does not depend on the gate length of the transistor **709**. Thus, it is possible to increase the gate

length of the transistor **709** without influencing the area of the ferroelectric memory cell **708**.

In the seventh embodiment, the line width **b2** of the plate line **701** including the storage nodes **704a** through **704h** in two lines satisfies the relationship $b2 < 2b1 + c1$.

Therefore, the length L7 of the ferroelectric memory cell **708** in the bit line direction according to the seventh embodiment satisfies $L7 = a1 + b2 < a1 + 2b1 + c1$.

Actually, the length of the ferroelectric memory cell **708** in the word line direction according to the seventh embodiment is set at a half of the length W12 of the ferroelectric memory cell **28** in the word line direction according to the second conventional example. Thus, if the length of the ferroelectric memory cell **28** in the word line direction according to the second conventional example is denoted by W12 and the area of the ferroelectric memory cell **28** is denoted by S12, the area S7 of the ferroelectric memory cell **708** according to the seventh embodiment satisfies the relationship:

$$
\begin{aligned}
S7 &= (a1 + b2) \times W12/2 \\
&< (a1 + 2b1 + c1) \times W12/2 \\
&< (a1/2 + b1 + c1/2) \times W12 = S12.
\end{aligned}
$$

Therefore, the area of the ferroelectric memory cell **708** according to the seventh embodiment can be smaller than the area of the ferroelectric memory cell **28** according to the second conventional example.

(Eighth embodiment)

Hereinafter, a ferroelectric memory according to the eighth embodiment will be described with reference to FIGS. **20** and **21**.

FIGS. **20** and **21** show a layout of a ferroelectric memory cell array according to the eighth embodiment. Note that FIG. **21** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **20**.

Referring to FIGS. **20** and **21**, the reference characters **801a**, **801b**, **801c** and **801d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **802a** and **802d** denote first word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **802b** and **802c** denote second word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **803a**, **803b**, **803c**, **803d**, **803e**, **803f**, **803g** and **803h** denote bit lines made of aluminum interconnections, the reference characters **804a**, **804b**, **804c**, **804d**, **804e**, **804f**, **804g** and **804h** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference characters **808a** and **808b** denote one-bit ferroelectric memory cells of the one-transistor one-capacitor type, the reference characters **809a** and **809b** denote transistors included in the ferroelectric memory cell **808**, and the reference character **810** denotes a short-channel transistor. Further, the reference characters **805a** and **805b** denote storage node contacts for connecting the storage nodes **804a** and **804b** and active regions **806a** and **806b** of the transistors **809a** and **809b**, respectively, and the reference characters **807a** and **807b** denote bit line contacts for connecting the bit lines **803a** through **803h** and the active regions **806a** and **806b** of the transistors **809a** and **809b**.

Referring to FIG. **20**, the reference character **a2** denotes the first inter-plate-line distance between the adjacent plate lines **801b** and **801c** with the bit line contacts **807** located therebetween, **b1** denotes the line width of the plate lines **801a** through **801d** including the storage nodes **804a** through **804h**, **c1** denotes the second inter-plate-line distance between the adjacent plate lines **801a** and **801b** without the bit line contacts **807** located therebetween, **d** denotes the distance between one side edge of the second word line **802b** and the center of the bit line contacts **807a** and **807b**, **e** denotes the line width of the second word line **802b**, and **f** denotes the distance between the other side edge of the

second word line **802b** and the center of the storage node contact **805b**. Note that the first inter-plate-line distance **a2** is not the shortest distance obtainable by machining of the plate lines **801b** and **801c**.

As shown in FIG. **20**, the storage nodes **804a** and **804b** of the ferroelectric capacitors of a pair of the ferroelectric memory cells **808a** and **808b** adjacent to each other in the word line direction are placed so as to be offset from each other in the bit line direction.

Note that the length of the ferroelectric memory cells **808a** and **808b** in the word line direction is set at a half of that of the ferroelectric memory cell **28** in the word line direction according to the second conventional example.

The plate lines **801a** and **801b** are provided for the respective storage nodes **804a** and **804b** of the ferroelectric memory cells adjacent to each other in the word line direction.

The active region **806a** of the transistor **809a**, included in one ferroelectric memory cell **808a** of the pair of the ferroelectric memory cells **808a** and **808b** adjacent to each other in the word line direction, extends in the bit line direction between the storage nodes of the ferroelectric capacitors included in the other ferroelectric memory cell **808b**, so as to intersect with the plate line **801b** for the other ferroelectric memory cell **808b**; on the other hand, the active region **806b** of the transistor **809b** included in the other ferroelectric memory cell **808b** does not intersect with the plate line **801a** for said one ferroelectric memory cell **808a**.

The first word line **802a** corresponds to the transistor **809a** included in said one ferroelectric memory cell **808a**, and the second word line **802b** corresponds to the transistor **809b** included in the other ferroelectric memory cell **808b**.

The second word line **802b** is formed to have a small width at its portion

intersecting with the active region **806a** of the transistor **809a** included in said one ferroelectric memory cell **808a** to a degree that does not put the active region **806a** into the OFF state, thereby forming the short-channel transistor **810**.

Thus, said one ferroelectric memory cell **808a** has the normal transistor **809a** and the short-channel transistor **810**. In this case, since the source-drain impedance of the short-channel transistor **810** is low, the influence of the short-channel transistor **810** on the operation of said one ferroelectric memory cell **808a** is negligible.

Furthermore, by using the short-channel transistor **810**, the active region **806a** intersects with the second word line **802b** that is different from the first word line **802a** for the transistor **809a** connected with the storage node **804a** of said one ferroelectric memory cell **808a**.

The length L8 of the ferroelectric memory cells **808a** and **808b** in the bit line direction according to the eighth embodiment satisfies $L8 = d + e + f + b1/2 + c1 + b1 + c1/2$.

The length of the ferroelectric memory cells **808a** and **808b** in the word line direction according to the eighth embodiment is a half of the length W12 of the ferroelectric memory cell **28** in the word line direction according to the second conventional example, and therefore, the area S8 of the ferroelectric memory cells **808a** and **808b** satisfies

$$S8 = (d + e + f + b1/2 + c1 + b1 + c1/2) \times W12/2.$$

Since the relationship $d + e + f > b1/2 + c1/2$ holds true, the following relationship is satisfied.

$$S8 < (2d + 2e + 2f + b1 + c1) \times W12/2$$

$$< (d + e + f + b1/2 + c1/2) \times W12$$

= S12 (area of the ferroelectric memory cell **28** according to the second

conventional example)

Thus, the area of the ferroelectric memory cells **808a** and **808b** according to the eighth embodiment can be made smaller than the area of the ferroelectric memory cell **28** according to the second conventional example.

(Ninth embodiment)

Hereinafter, a ferroelectric memory according to the ninth embodiment will be described with reference to FIGS. **22**, **23** and **24**.

FIGS. **22** and **23** show a layout of a ferroelectric memory cell array according to the ninth embodiment, and FIG. **24** shows a cross-sectional structure taken along the line **C-C** of FIGS. **22** and **23**. Note that FIG. **23** shows only active regions, word lines, bit line contacts and storage node contacts extracted from the layout shown in FIG. **22**.

Referring to FIGS. **22**, **23** and **24**, the reference characters **901a**, **901b**, **901c** and **901d** denote plate lines constructed of upper electrodes of ferroelectric capacitors, the reference characters **902a**, **902b** and **902c** denote word lines made of polycrystalline silicon and constructed of gate electrodes of access transistors, the reference characters **903a**, **903b**, **903c** and **903d** denote bit lines constructed of active regions, the reference characters **904a**, **904b**, **904c** and **904d** denote storage nodes of ferroelectric memory cells, each constructed of a lower electrode of the ferroelectric capacitor, the reference character **908** denotes a one-bit ferroelectric memory cell of the one-transistor one-capacitor type, and the reference character **909** denotes a transistor included in the ferroelectric memory cell **908**. Further, the reference character **905** denotes storage node contacts for connecting the storage nodes **904a** through **904d** and the bit lines **903a** through **903d** constructed of the active regions.

Referring to FIG. **22**, the reference character **b1** denotes the line width of the plate lines **901a** through **901d** including the storage nodes **904a** through **904d**, and **c1** denotes

the distance between the adjacent plate lines **901a** and **901b** without bit line contacts located therebetween.

The bit lines are formed integrally with the active regions of the transistors **909** of the ferroelectric memory cells **908** arranged in the bit line direction, and are running in the bit line direction between the storage nodes **904a** through **904d** of the ferroelectric capacitors of pairs of the ferroelectric memory cells **908** adjacent to each other in the word line direction.

The word lines **902a** through **902c** are provided in common for the transistors **909** of the ferroelectric memory cells **908** arranged in the word line direction. Furthermore, each of the word lines **902a** through **902c** has: interconnection portions, each having a small width that does not put the bit lines **903a** through **903d** into the OFF state, which are formed above the bit lines **903a** through **903d**; and gate electrode portions which are formed above the active regions of the transistors **909**, and are wider than the interconnection portions each having a small width.

In the ninth embodiment, the bit lines **903a** through **903d** are constructed of the active regions; therefore, unlike the case of the bit lines made of aluminum interconnections, it is unnecessary to provide bit line contacts for connecting the bit lines with the active regions.

The length L9 of the ferroelectric memory cell **908** in the bit line direction according to the ninth embodiment satisfies $L9 = b1 + c1$.

Since the relationship $d + e + f > c1/2 + b1/2$ holds true, the following relationship is satisfied.

$$
\begin{aligned}
L9 &= (b1/2 + c1/2) + (b1/2 + c1/2) \\
&< d + e + f + (b1/2 + c1/2) \\
&= L12 \text{ (length of the ferroelectric memory cell } \mathbf{28} \text{ in the bit line direction}
\end{aligned}
$$

according to the second conventional example)

Thus, the area of the ferroelectric memory cell **908** according to the ninth embodiment can be made smaller than the area of the ferroelectric memory cell **28** according to the second conventional example.

[Effects of the Invention]

In each of the first through fourth ferroelectric memories according to the present invention, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the first conventional example.

Furthermore, in each of the fifth through ninth ferroelectric memories according to the present invention, the length of each memory cell in the bit line direction can be made small even if the gate length of each transistor is set equal to that of each transistor in the second conventional example; therefore, the area of each memory cell and thus the area of the memory cell array can be reduced compared with the second conventional example.

[Brief Description of the Drawings]

[FIG. **1**]

A layout of a ferroelectric memory according to the first embodiment.

[FIG. **2**]

A layout of the ferroelectric memory according to the first embodiment.

[FIG. **3**]

A cross-sectional view of the ferroelectric memory according to the first embodiment, taken along the line **A-A** of FIGS. **1** and **2**.

[FIG. **4**]

A layout of a ferroelectric memory according to a modification of the first embodiment.

[FIG. **5**]

A layout of a ferroelectric memory according to the second embodiment.

[FIG. **6**]

A layout of the ferroelectric memory according to the second embodiment.

[FIG. **7**]

A layout of a ferroelectric memory according to the third embodiment.

[FIG. **8**]

A layout of the ferroelectric memory according to the third embodiment.

[FIG. **9**]

A layout of a ferroelectric memory according to the fourth embodiment.

[FIG. **10**]

A layout of the ferroelectric memory according to the fourth embodiment.

[FIG. **11**]

A layout of a ferroelectric memory according to a modification of the fourth embodiment.

[FIG. **12**]

A layout of a ferroelectric memory according to the fifth embodiment.

[FIG. **13**]

A layout of the ferroelectric memory according to the fifth embodiment.

[FIG. **14**]

A cross-sectional view of the ferroelectric memory according to the fifth embodiment, taken along the line **B-B** of FIGS. **13** and **14**.

[FIG. **15**]

A layout of a ferroelectric memory according to the sixth embodiment.

[FIG. **16**]

A layout of the ferroelectric memory according to the sixth embodiment.

[FIG. **17**]

A layout of the ferroelectric memory according to the sixth embodiment.

[FIG. **18**]

A layout of a ferroelectric memory according to the seventh embodiment.

[FIG. **19**]

A layout of the ferroelectric memory according to the seventh embodiment.

[FIG. **20**]

A layout of a ferroelectric memory according to the eighth embodiment.

[FIG. **21**]

A layout of the ferroelectric memory according to the eighth embodiment.

[FIG. **22**]

A layout of a ferroelectric memory according to the ninth embodiment.

[FIG. **23**]

A layout of the ferroelectric memory according to the ninth embodiment.

[FIG. **24**]

A cross-sectional view of the ferroelectric memory according to the ninth embodiment, taken along the line **C-C** of FIGS. **22** and **23**.

[FIG. **25**]

A diagram showing a circuit configuration of a ferroelectric memory according to the first and second conventional examples and the first through ninth embodiments.

[FIG. **26**]

A layout of the ferroelectric memory according to the first conventional example.

[FIG. **27**]

A layout of the ferroelectric memory according to the first conventional example.

[FIG. **28**]

A cross-sectional view of the ferroelectric memory according to the first conventional example, taken along the line **D-D** of FIGS. **26** and **27**.

[FIG. **29**]

A layout of the ferroelectric memory according to the second conventional example.

[FIG. **30**]

A layout of the ferroelectric memory according to the second conventional example.

[FIG. **31**]

A cross-sectional view of the ferroelectric memory according to the second conventional example, taken along the line **E-E** of FIGS. **29** and **30**.

[Description of the Reference Characters]

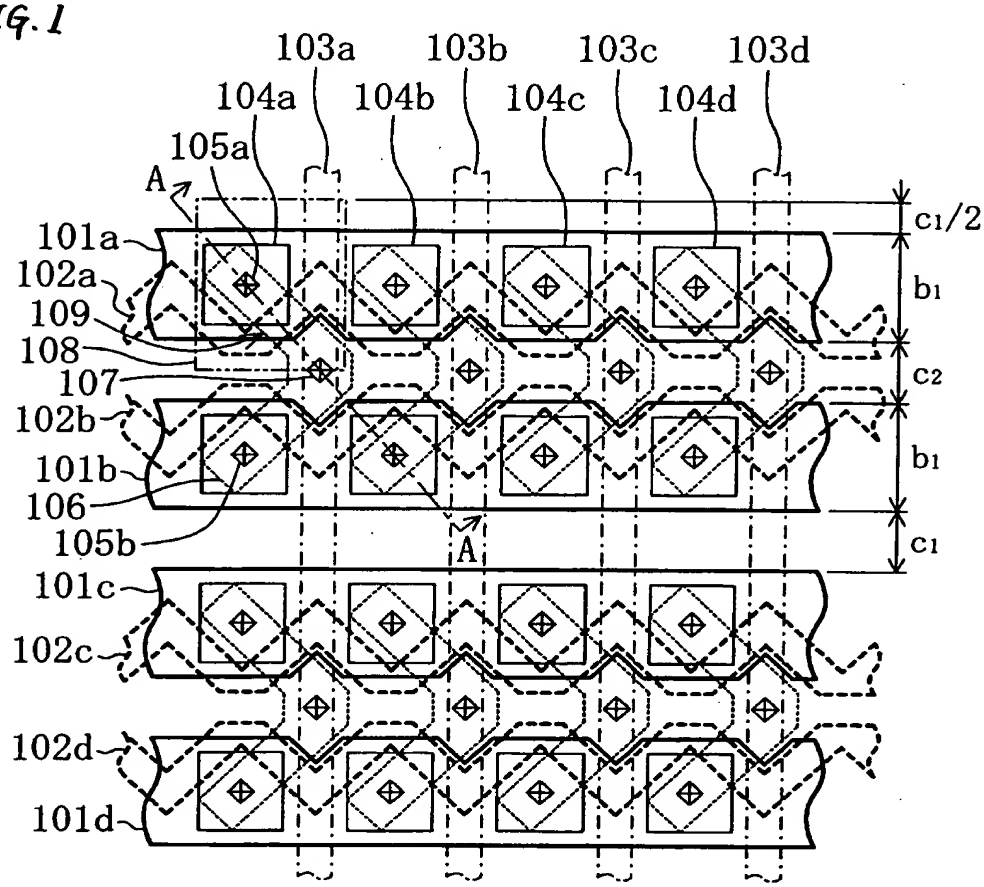
101a, 101b, 101c, 101d	plate line
102a, 102b, 102c, 102d	word line
103a, 103b, 103c, 103d	bit line
104a, 104b, 104c, 104d	storage node
105	storage node contact
106	active region
107	bit line contact
108	ferroelectric memory cell
109	transistor
201a, 201b	plate line
202a, 202b	word line
203a, 203b, 203c, 203d, 203e, 203f, 203g, 203h	bit line
204a, 204b, 204c, 204d, 204e, 204f, 204g, 204h	storage node

205	storage node contact
206	active region
207	bit line contact
208	ferroelectric memory cell
209a, 209b	transistor
301a, 301b, 301c, 301d	plate line
302a, 302b	word line
303a, 303b, 303c, 303d, 303e, 303f, 303g, 303h	bit line
304a, 304b, 304c, 304d, 304e, 304f, 304g, 304h	storage node
305	storage node
306	active region
307	bit line contact
308	ferroelectric memory cell
309a, 309b	transistor
401	plate line
402a, 402b	word line
403a, 403b, 403c, 403d, 403e, 403f, 403g, 403h	bit line
404a, 404b, 404c, 404d, 404e, 404f, 404g, 404h	storage node
405	storage node contact
406	active region
407	bit line contact
408	ferroelectric memory cell
409	transistor
501a, 501b, 501c, 501d	plate line
502a, 502b, 502c, 502d	word line

503a, 503b, 503c, 503d	bit line
504a, 504b, 504c, 504d	storage node
505	storage node contact
506	active region
507	bit line contact
508	ferroelectric memory cell
509	transistor
601a, 601b, 601c, 601d	plate line
602a, 602b, 602c, 602d	word line
603a, 603b, 603c, 603d	bit line
604a, 604b, 604c, 604d	storage node
605	storage node contact
606	active region
607	bit line contact
608	ferroelectric memory cell
609	transistor
701	plate line
702	word line
703a, 703b, 703c, 703d, 703e, 703f, 703g, 703h	bit line
704a, 704b, 704c, 704d, 704e, 704f, 704g, 704h	storage node
705	storage node contact
706	active region
707	bit line contact
708	ferroelectric memory cell
709	transistor

801a, 801b, 801c, 801d	plate line
802a, 802d	first word line
802c, 802c	second word line
803a, 803b, 803c, 803d, 803e, 803f, 803g, 803h	bit line
804a, 804b, 804c, 804d, 804e, 804f, 804g, 804h	storage node
805a, 805b	storage node contact
806a, 806b	active region
807a, 807b	bit line contact
808a, 808b	ferroelectric memory cell
809a, 809b	transistor
810	short-channel transistor
901a, 901b, 901c, 901d	plate line
902a, 902b, 902c	word line
903a, 903b, 903c, 903d	bit line (active region)
904a, 904b, 904c, 904d	storage node
905	storage node contact
908	ferroelectric memory cell
909	transistor

【書類名】　図面→ Drawings
↳ Name of the Document
【図１】
↓
FIG. 1



【図２】

FIG. 2

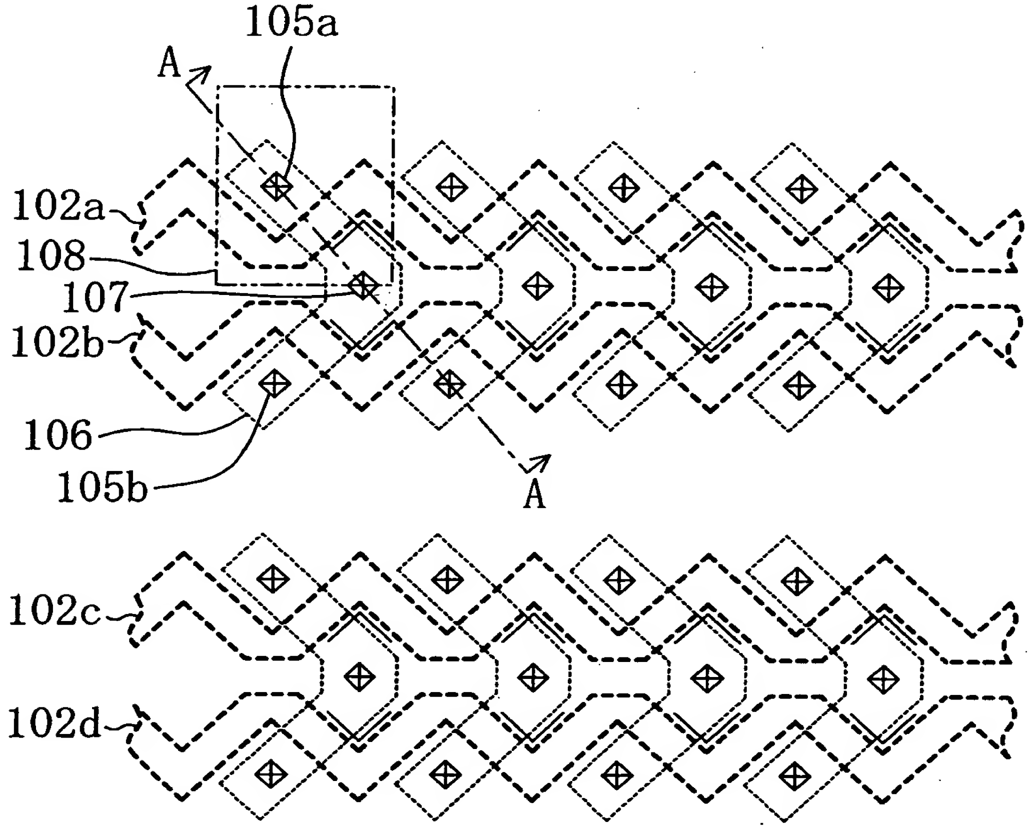


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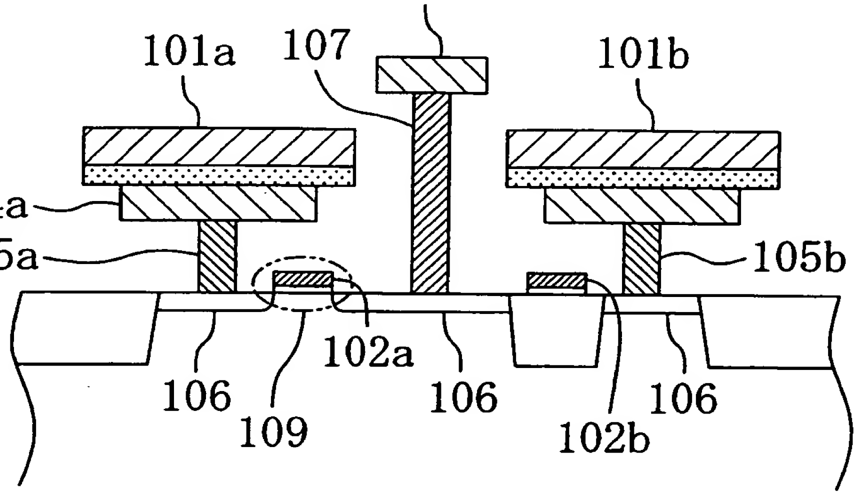
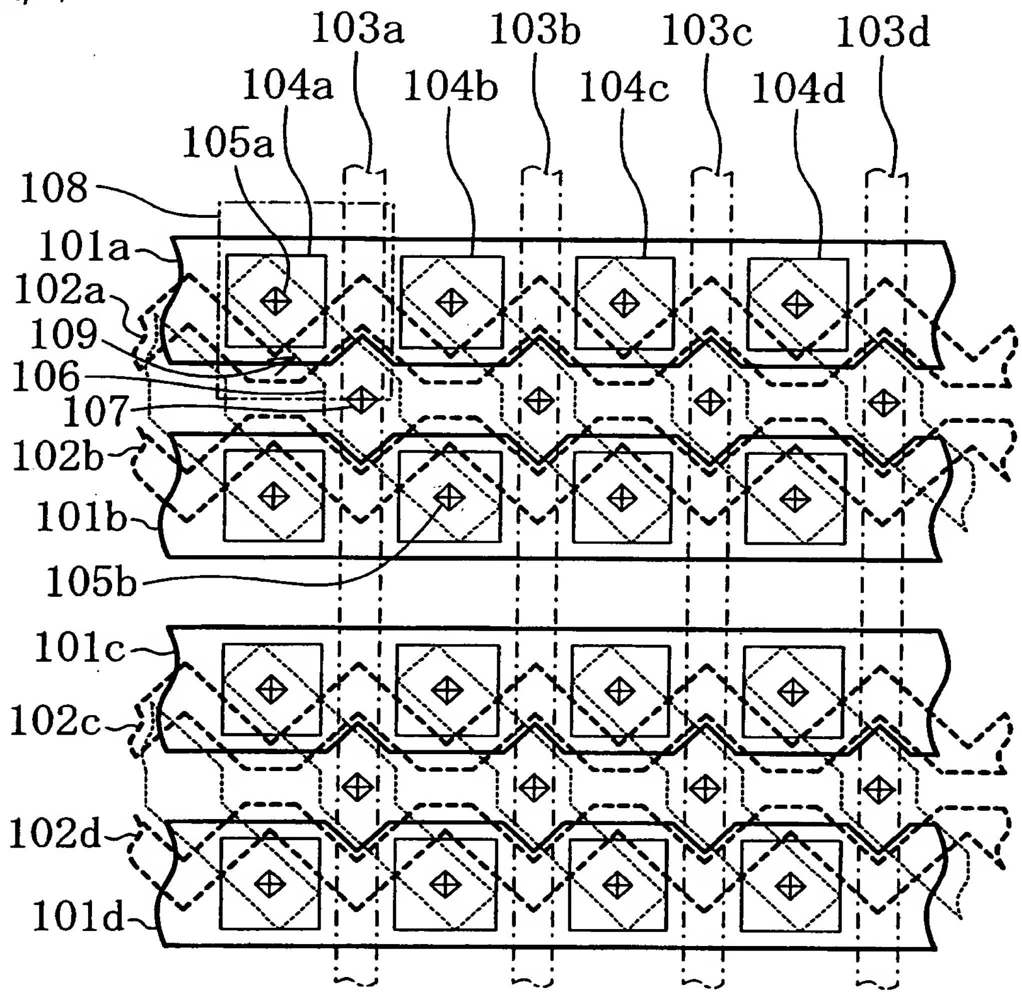
FIG. 3



【図４】

FIG. 4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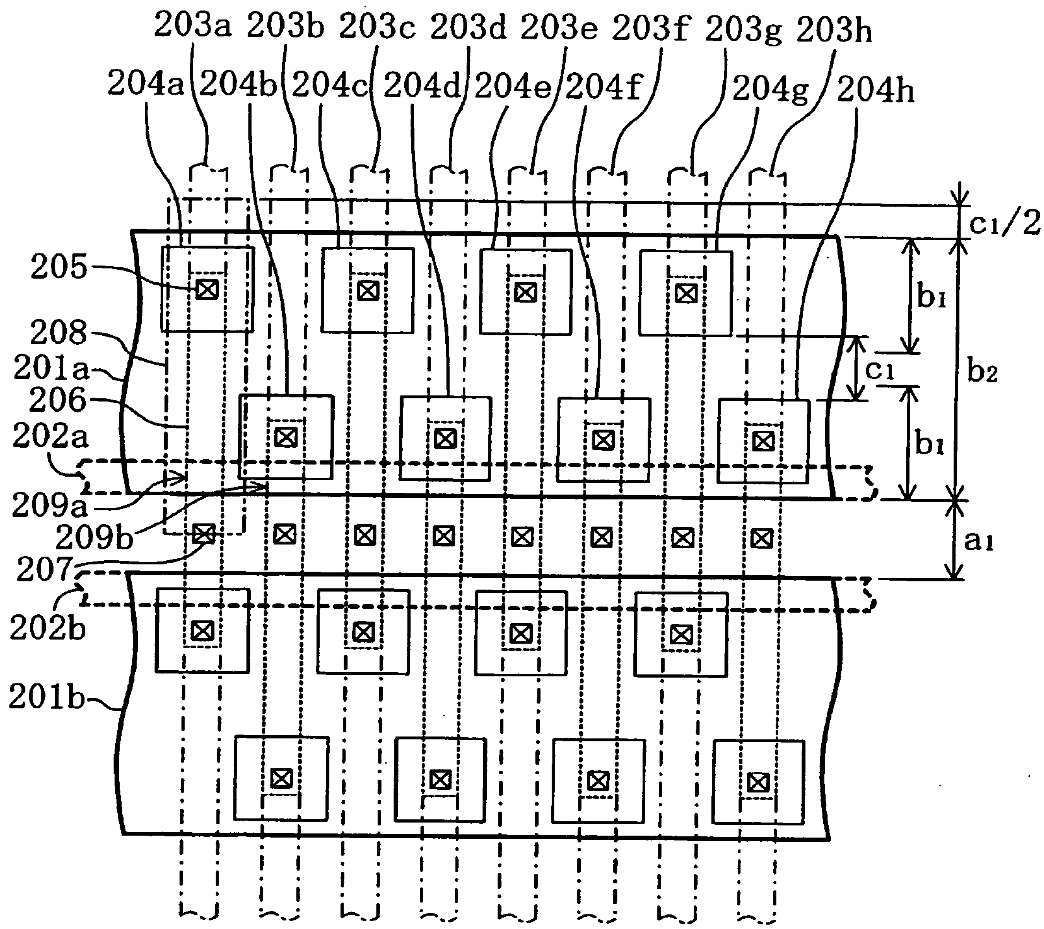
【図５】
↓
FIG. 5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204a 204b 204c 204d 204e 204f 204g 204h
205
208
201a
206
202a
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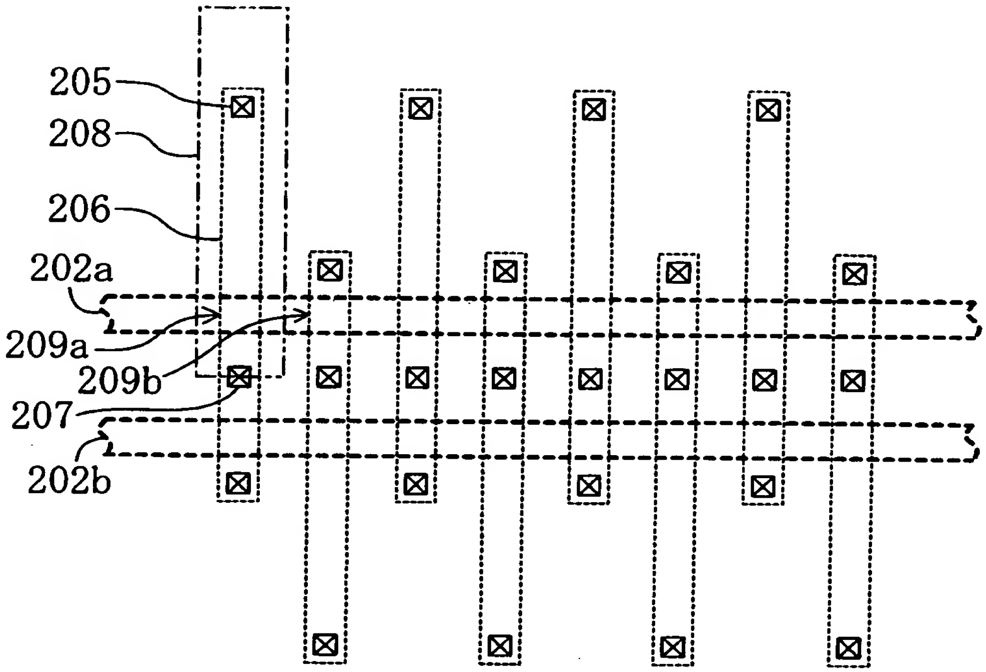
209b
207
202b
201b
c1/2
b1
c1
b2
b1
a1

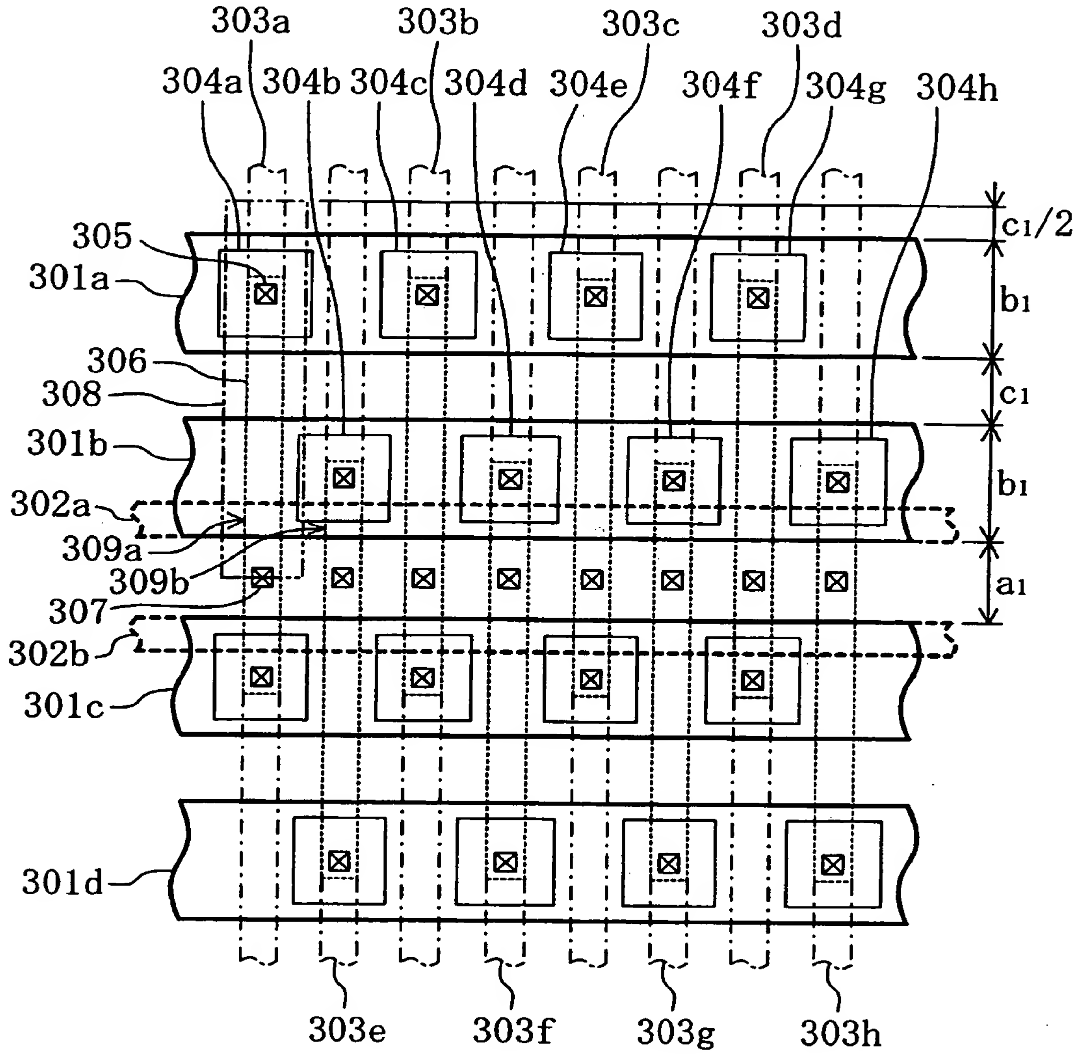
【図６】

FIG. 6



【図７】

FIG.7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302a
309a
309b
307
302b
301c
301d
c1/2
b1
c1
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303e
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【図８】

FIG. 8

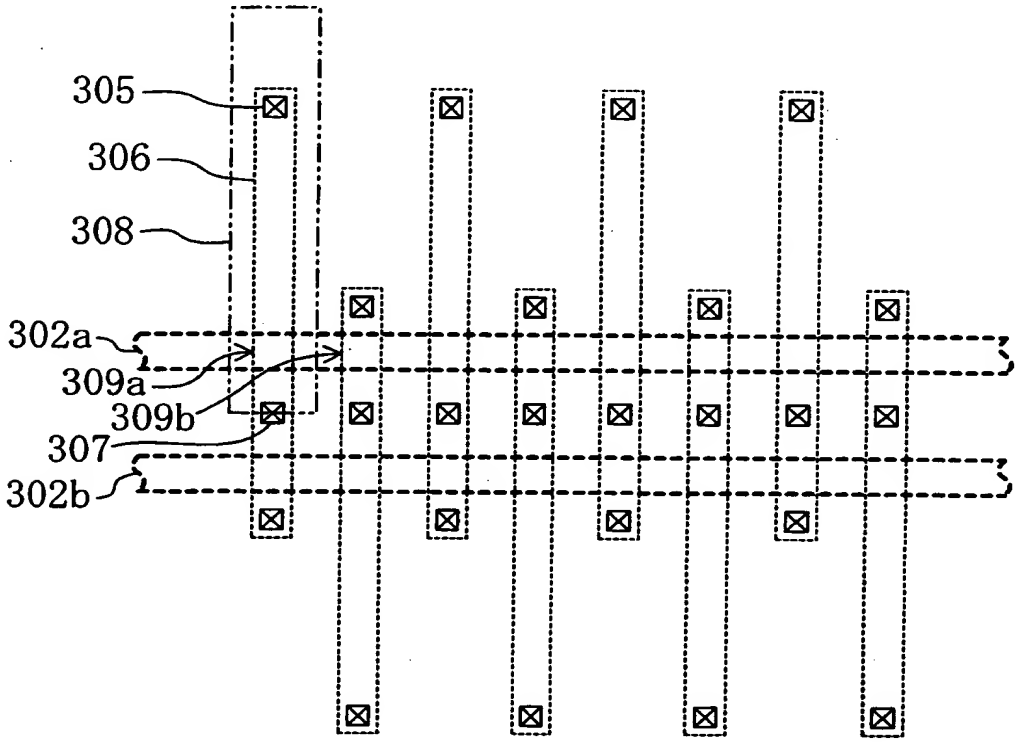

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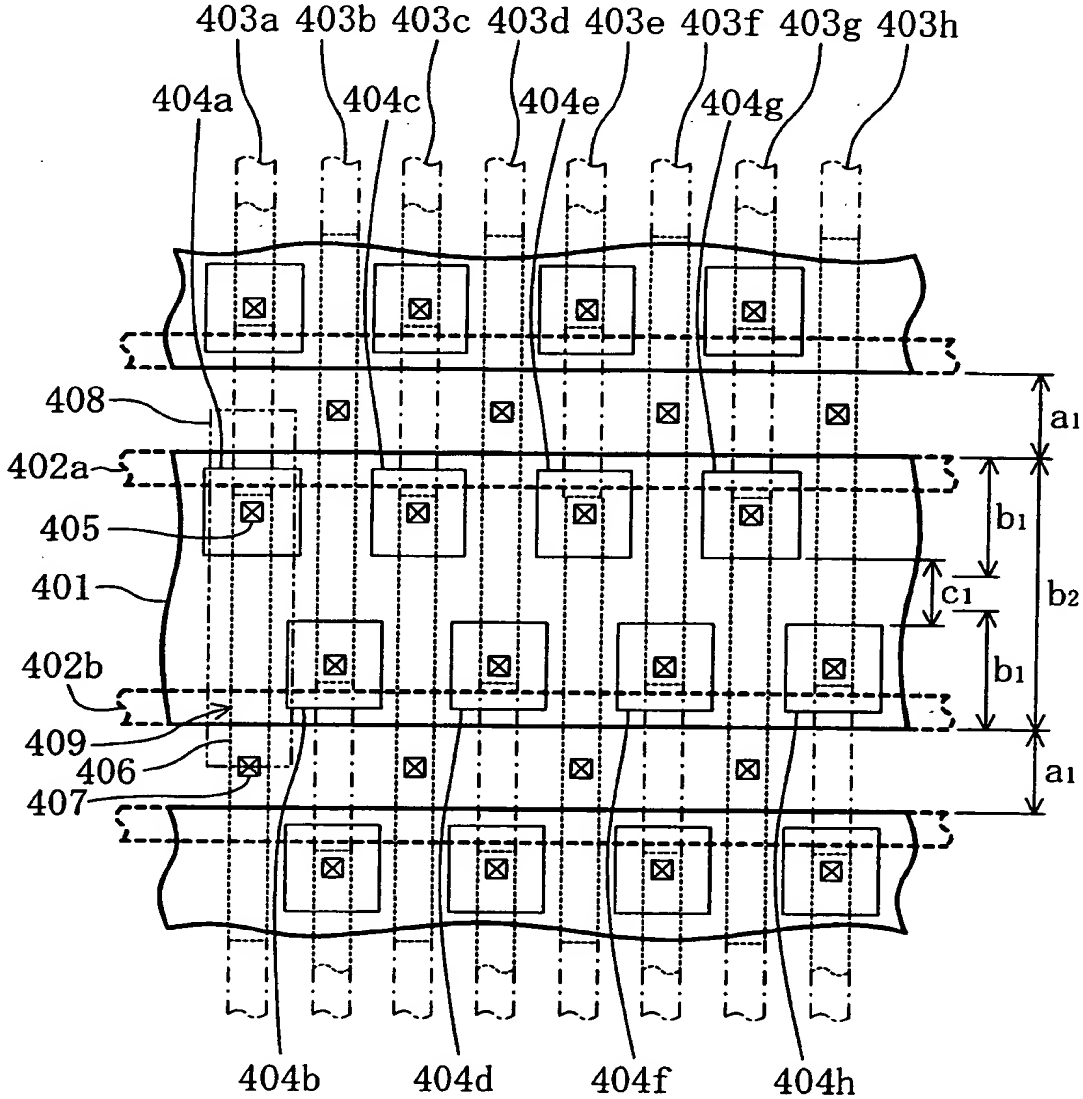
FIG. 9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403g
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404c
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402a
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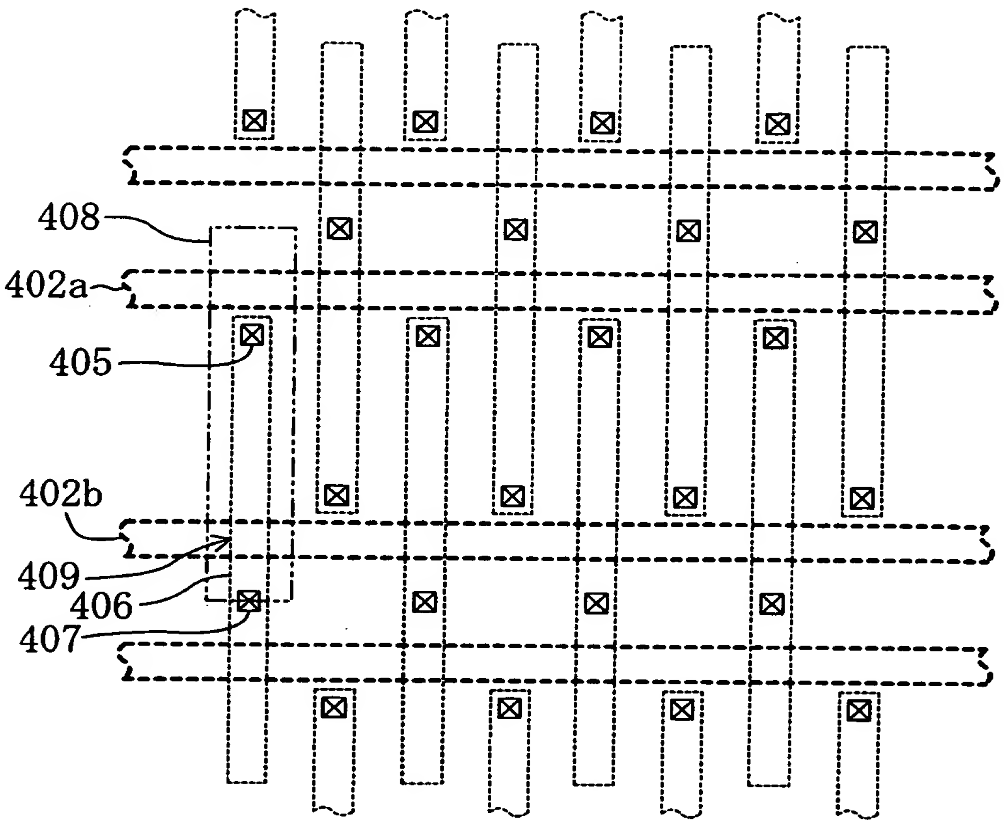
402b
409
406
407
a1
b1
c1
b2
b1
a1
404b
404d
404f
404h

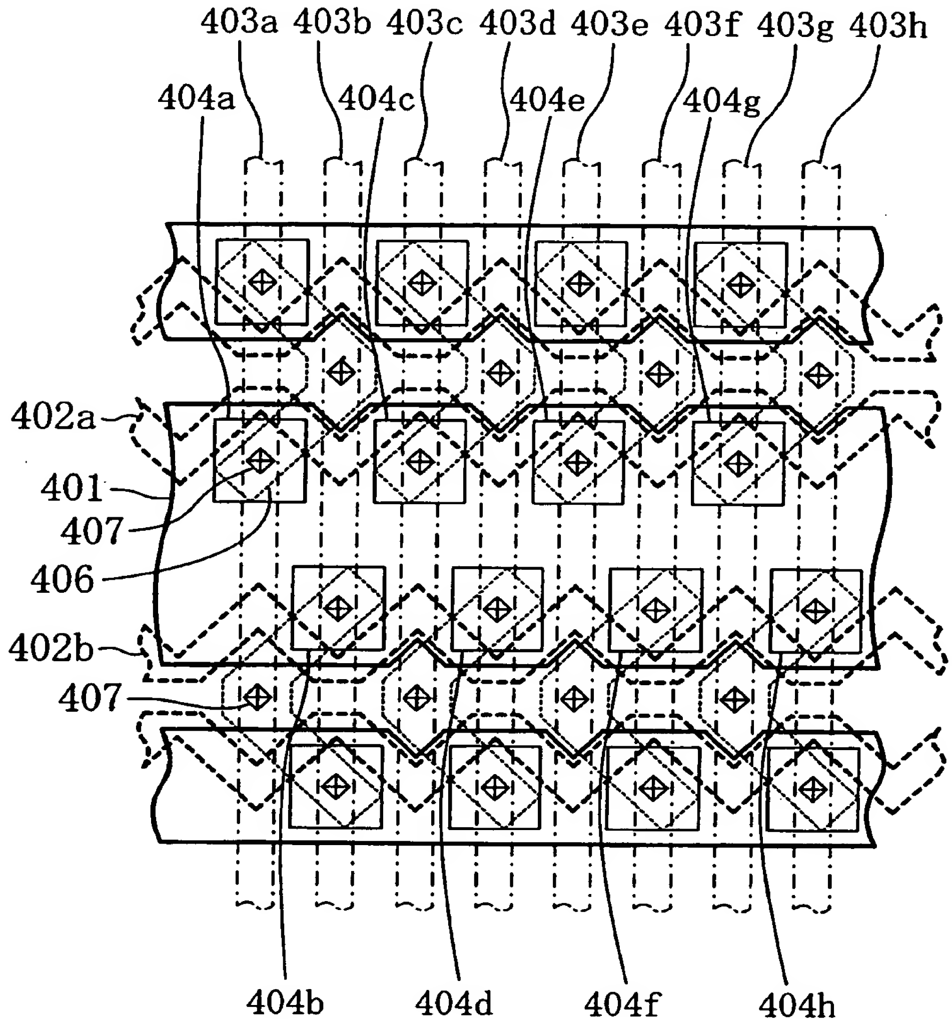
【図１０】

FIG. 10



【図１１】

FIG. 11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403e
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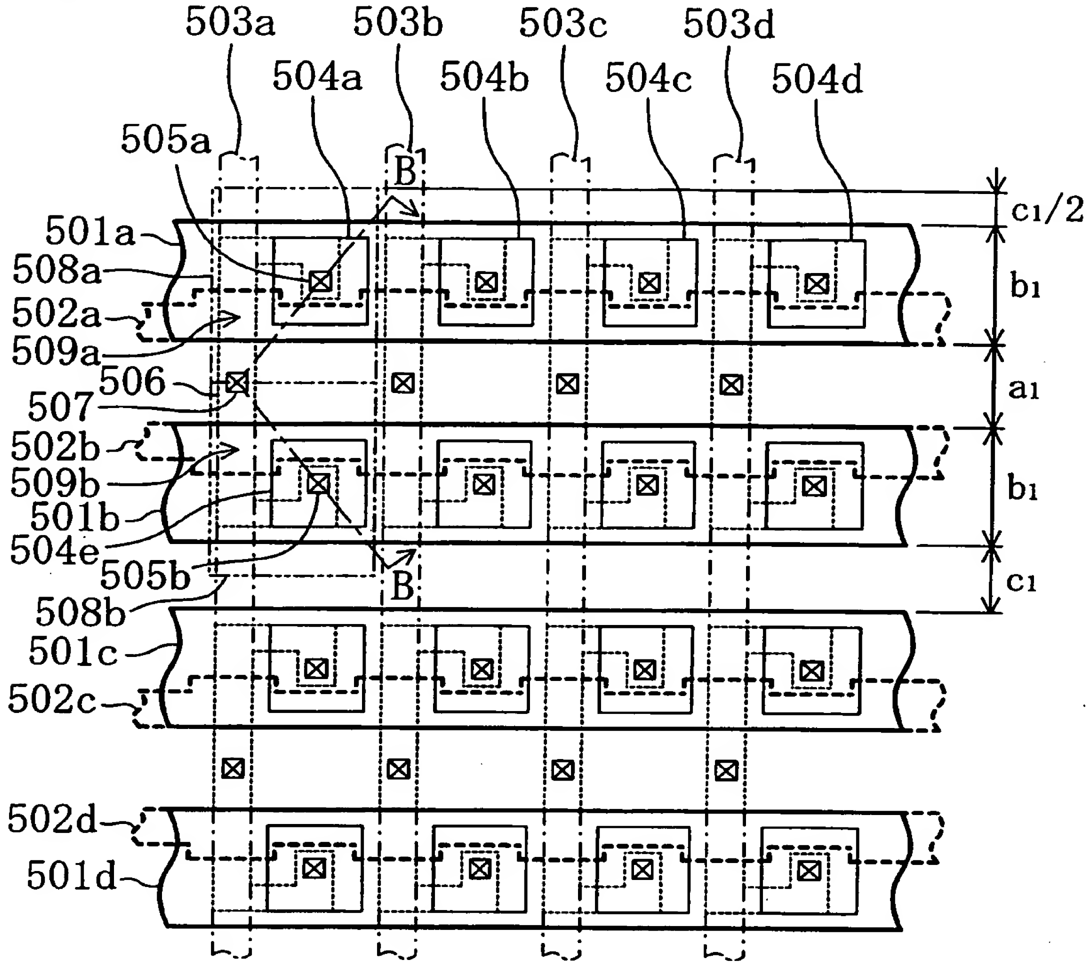
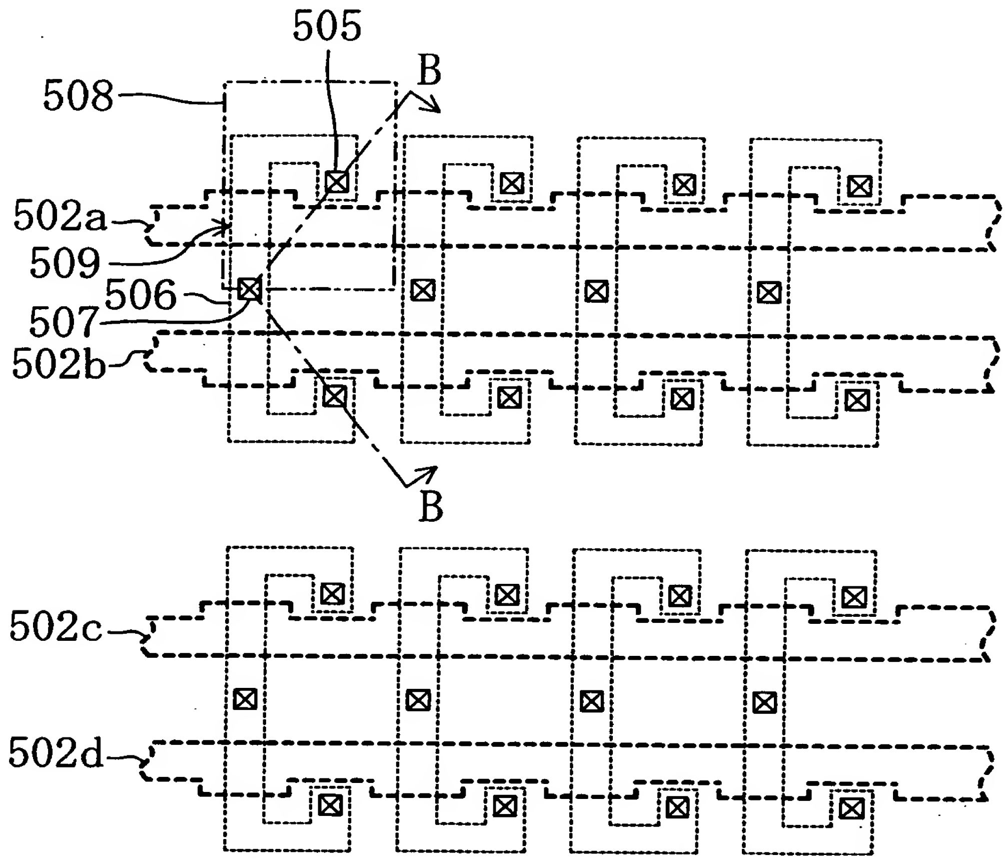
404e
404g
402a
401
407
406
402b
407
404b
404d
404f
404h

【図１２】

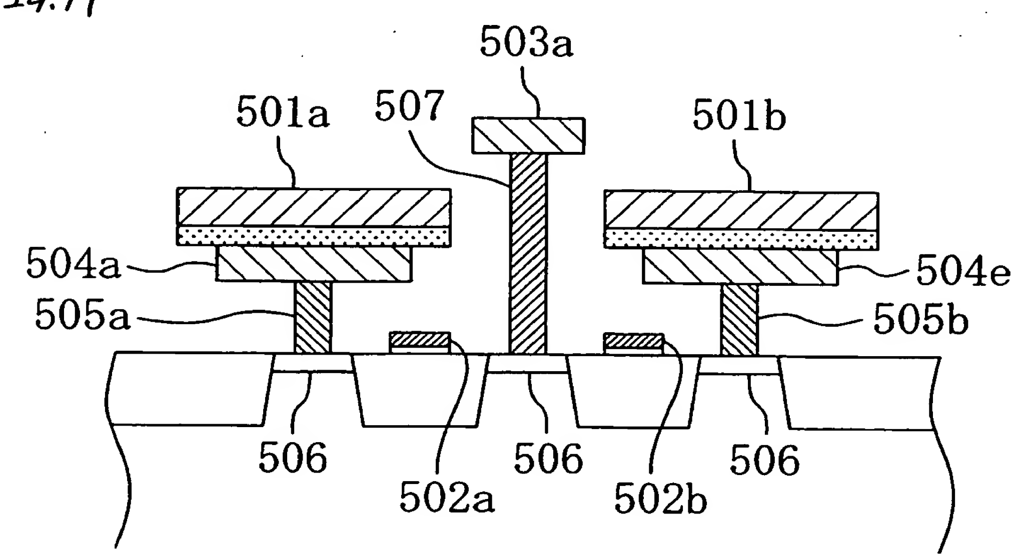
FIG. 12


503a
503b
503c
503d
504a
504b
504c
504d
505a
B
501a
508a
502a
509a
506
507
502b
509b
501b
504e
505b
508b
501c
502c
502d
501d
c1/2
b1
a1
b1
c1

【図１３】
FIG. 13

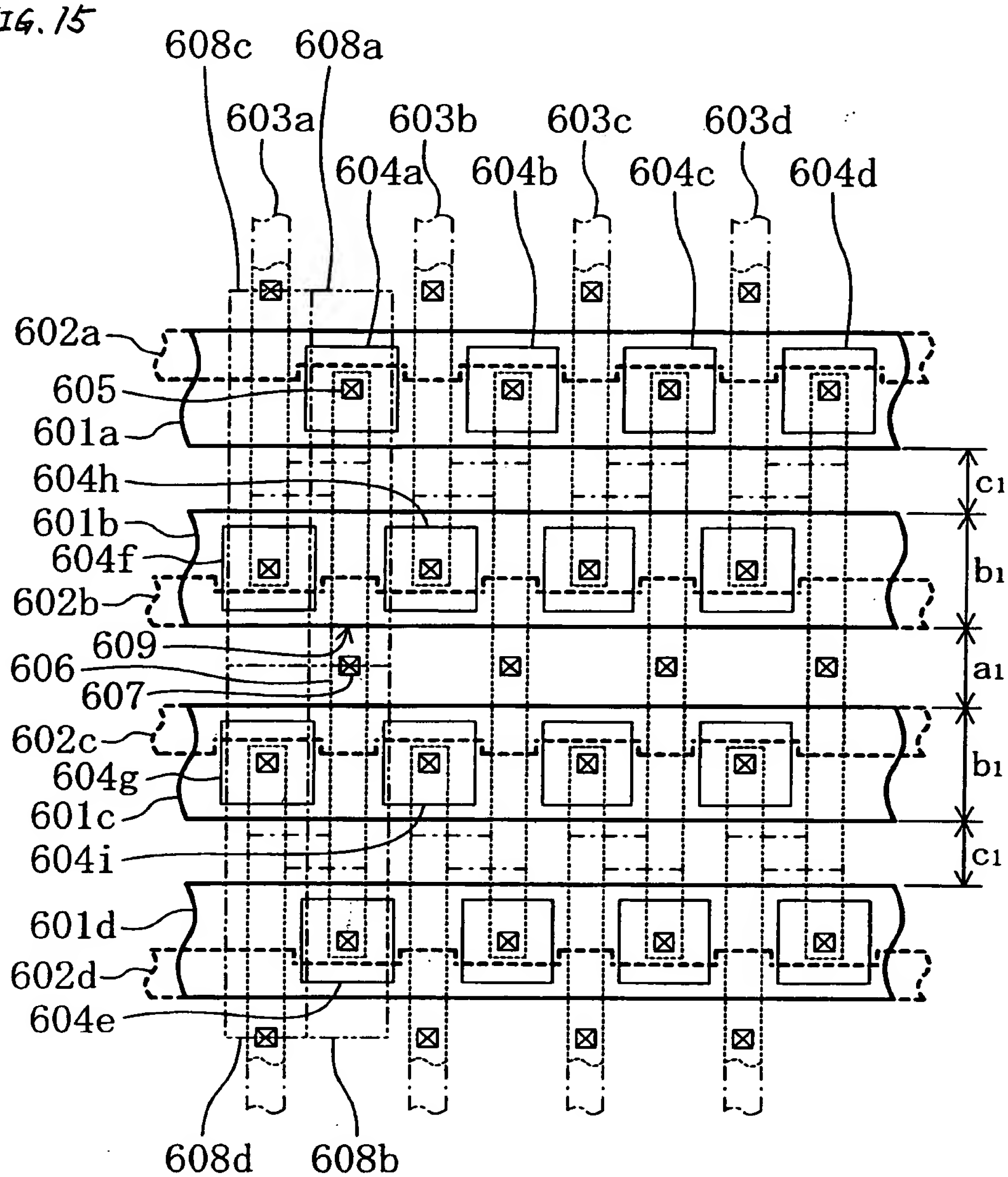


【図１４】
FIG. 14



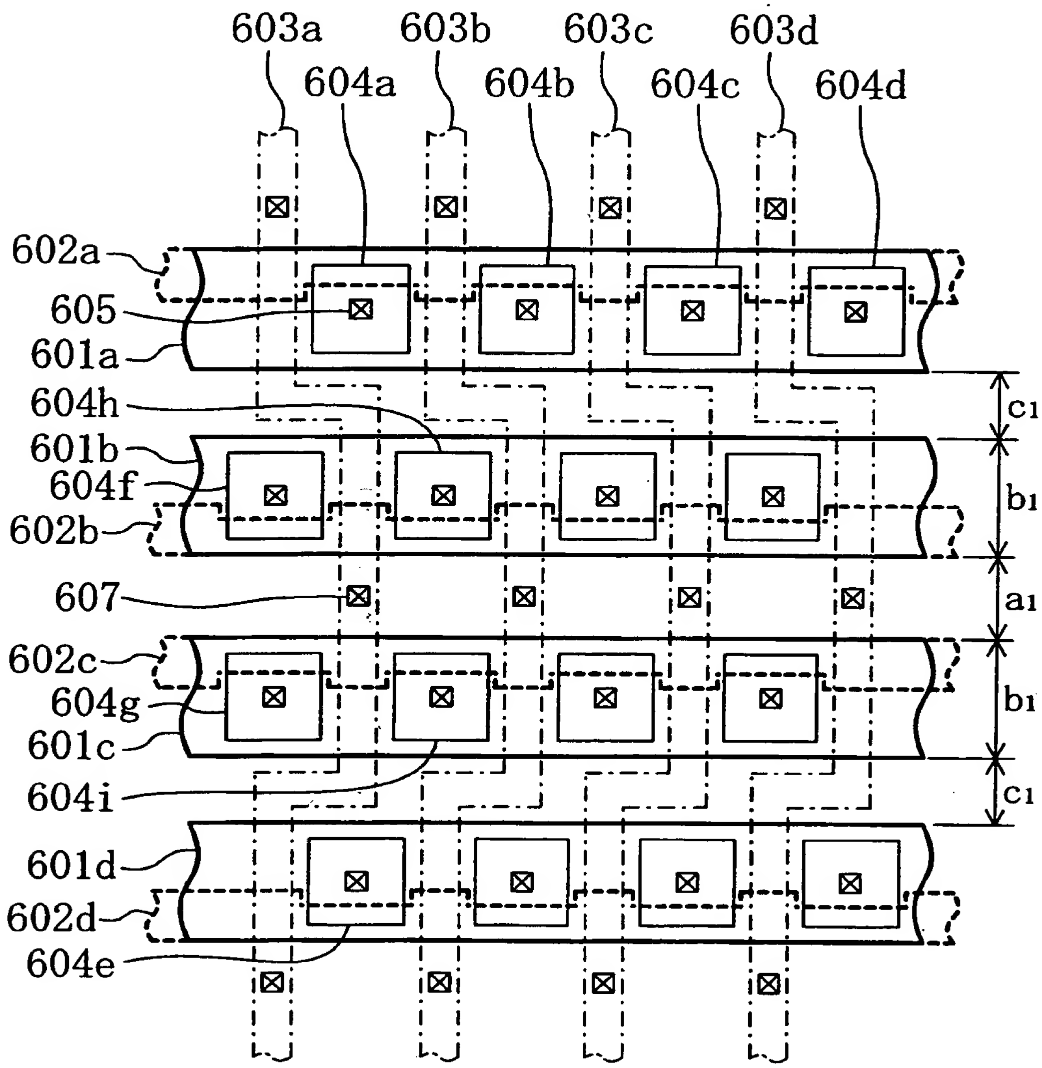
【図１５】

FIG. 15

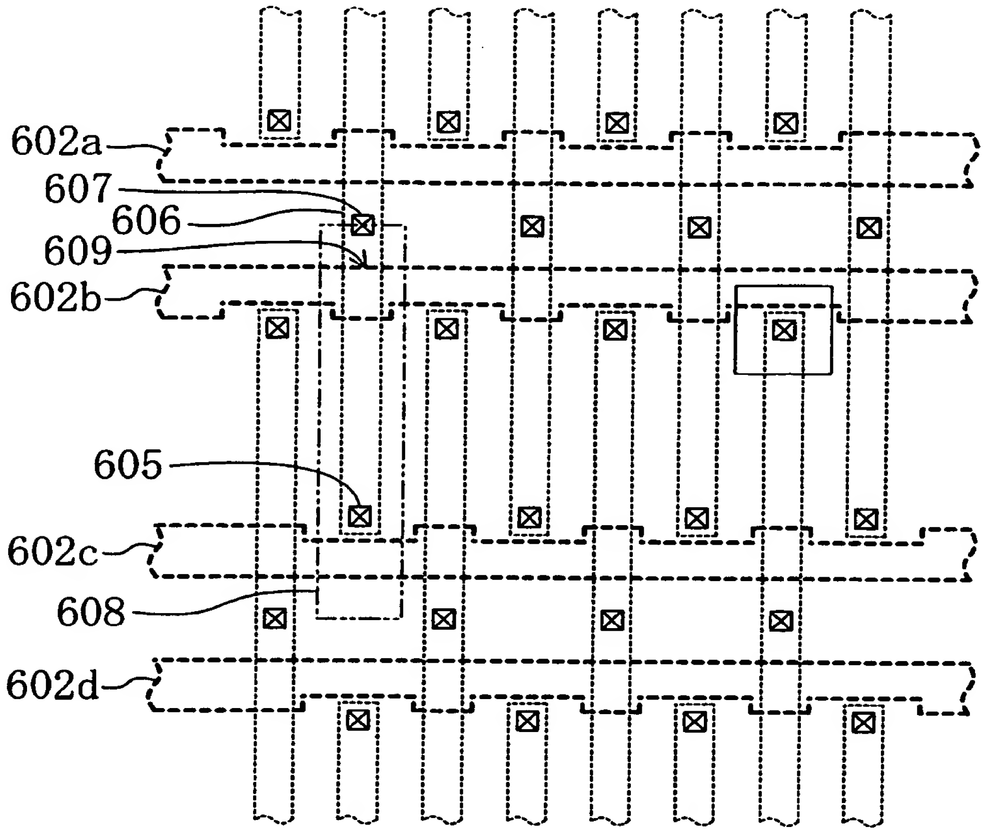

608c
608a
603a
603b
603c
603d
604a
604b
604c
604d
602a
605
601a
604h
601b
604f
602b
609
606
607
602c
604g
601c
604i
601d
602d
604e
608d
608b
c1
b1
a1
b1
c1

【図１６】

FIG.16

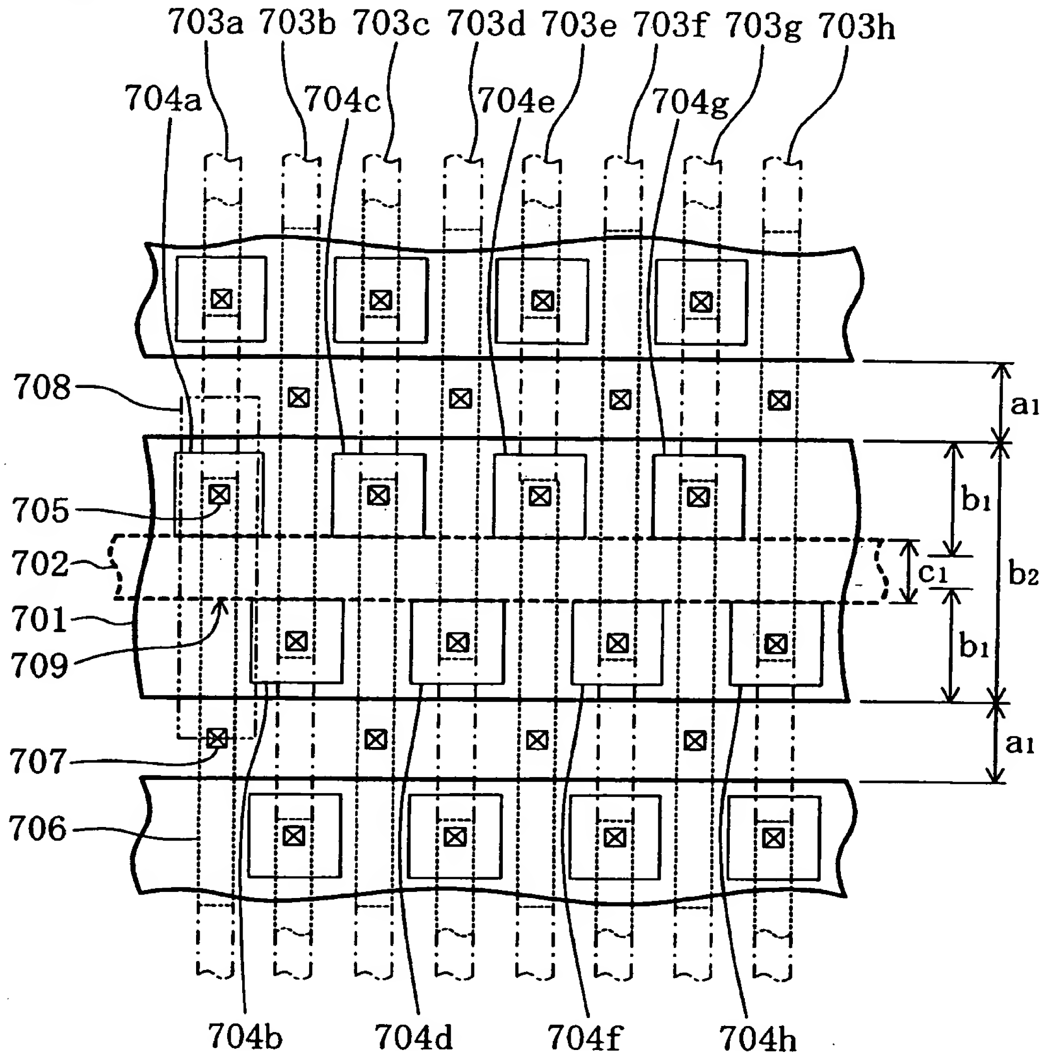

603a
603b
603c
603d
604a
604b
604c
604d
602a
605
601a
604h
601b
604f
602b
607
602c
604g
601c
604i
601d
602d
604e
c1
b1
a1
b1
c1

【図１７】
FIG. 17

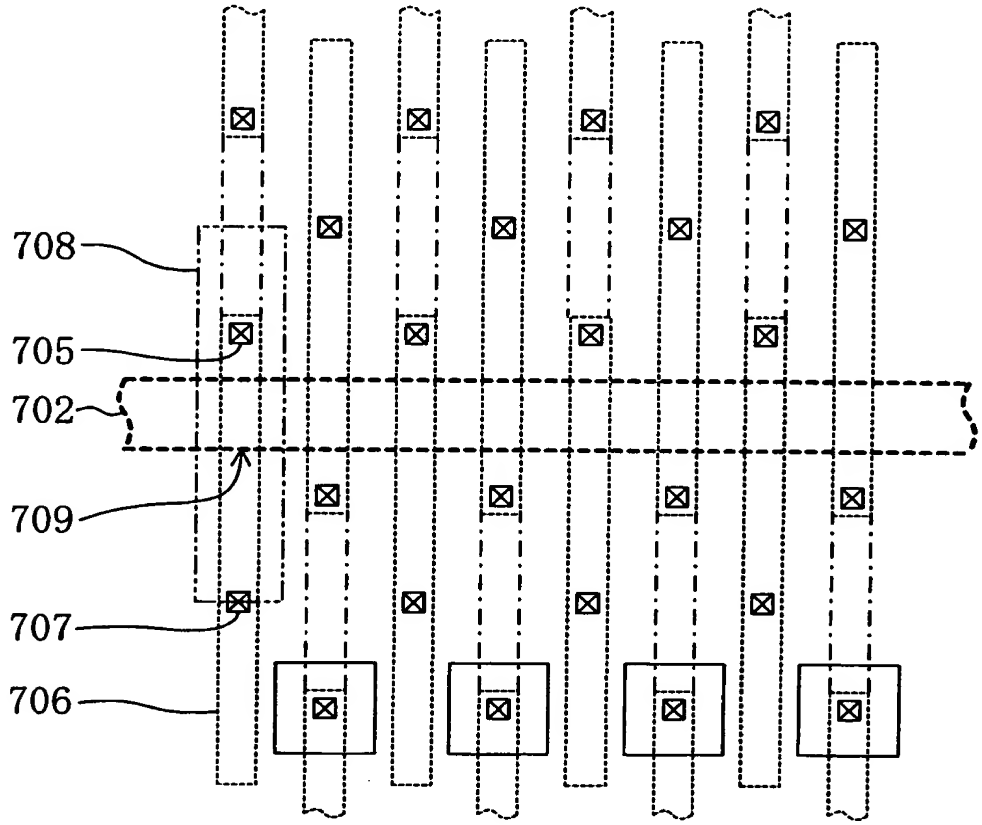


【図１８】

FIG.18

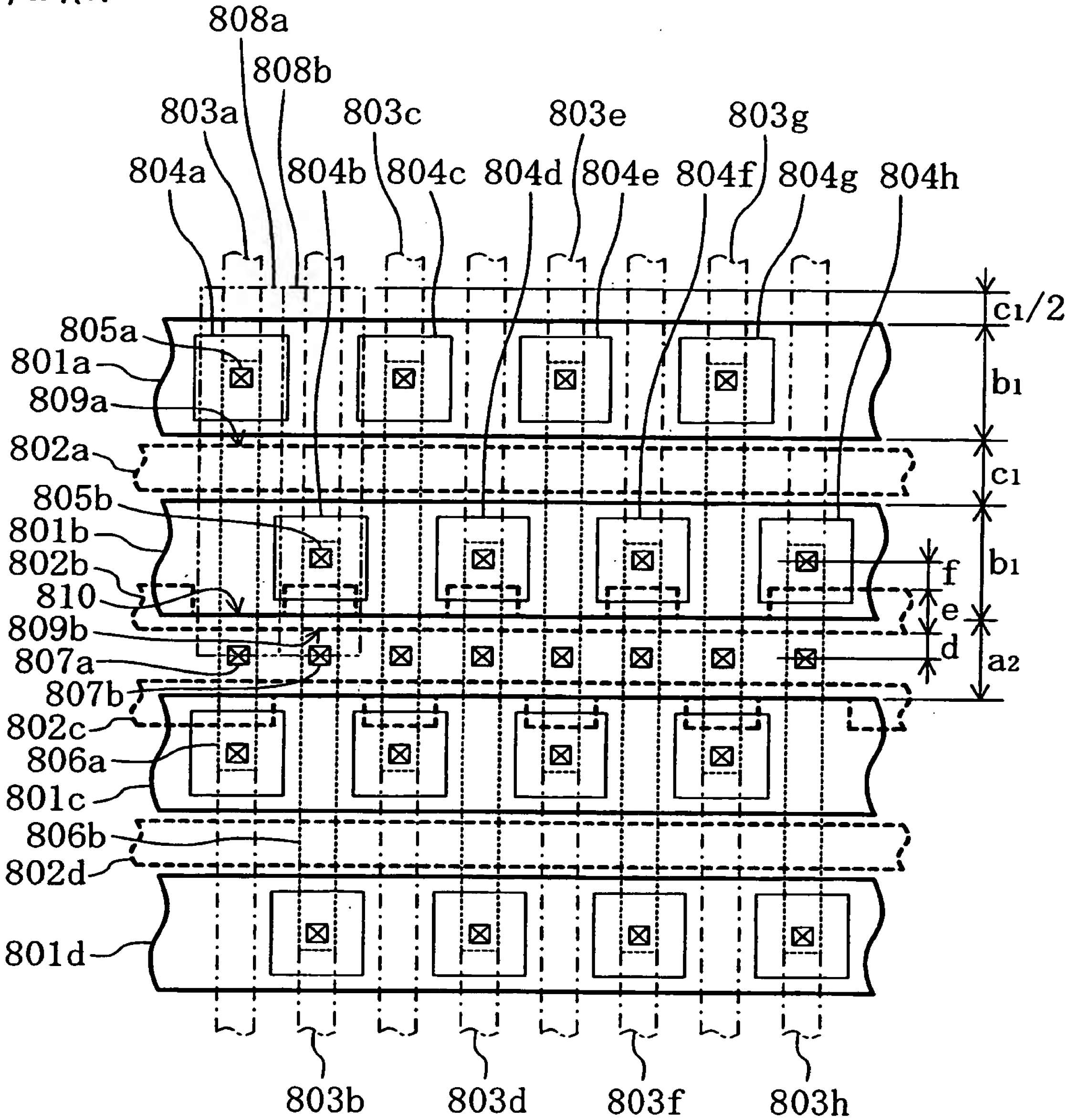

703a 703b 703c 703d 703e 703f 703g 703h
704a
704c
704e
704g
708
705
702
701
709
707
706
a1
b1
c1
b2
b1
a1
704b
704d
704f
704h

【図１９】
FIG. 19



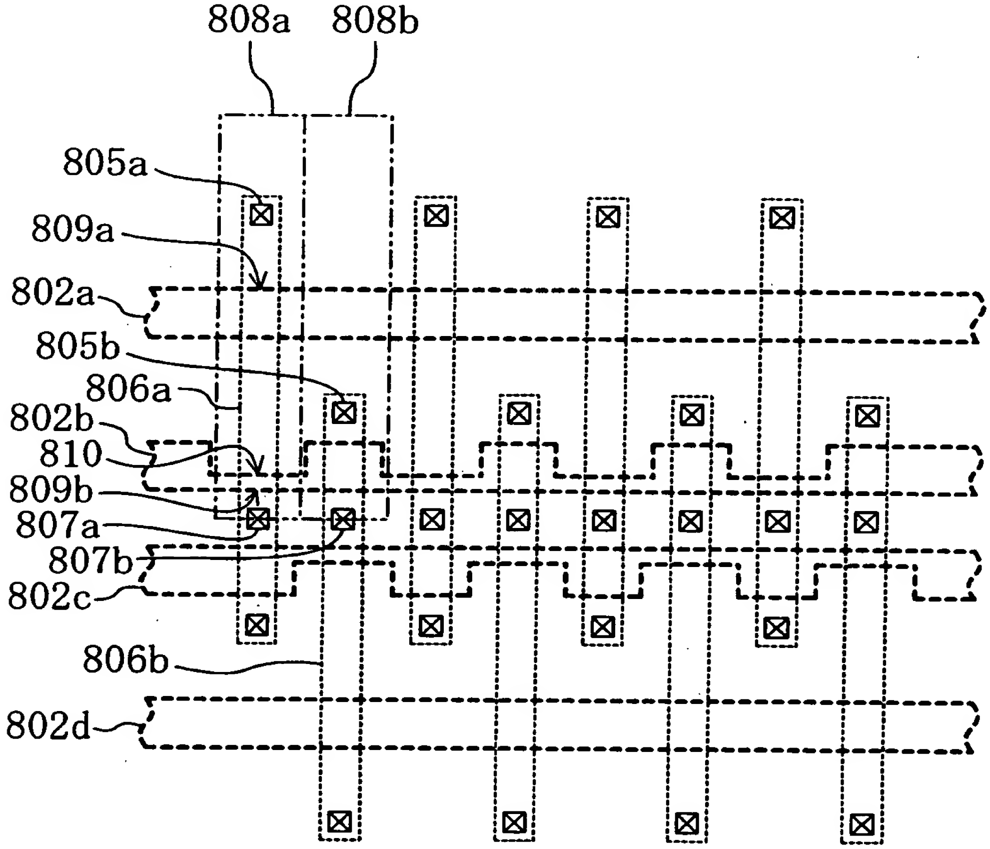
【図２０】

FIG.20


808a
808b
803a
803c
803e
803g
804a
804b
804c
804d
804e
804f
804g
804h
805a
801a
809a
802a
805b
801b
802b
810
809b
807a
807b
802c
806a
801c
806b
802d
801d
c1/2
b1
c1
b1
f
e
d
a2
803b
803d
803f
803h

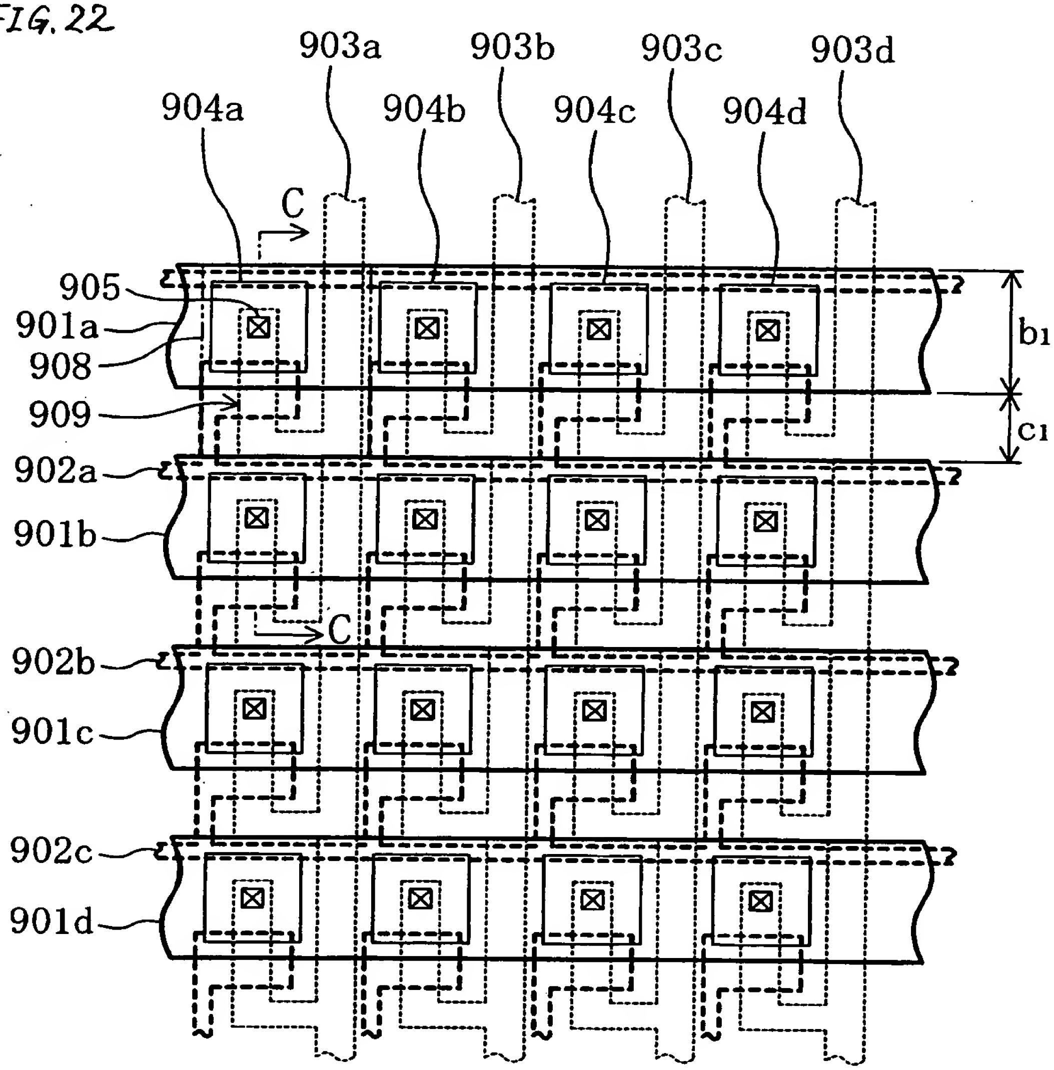
【図２１】

FIG. 21

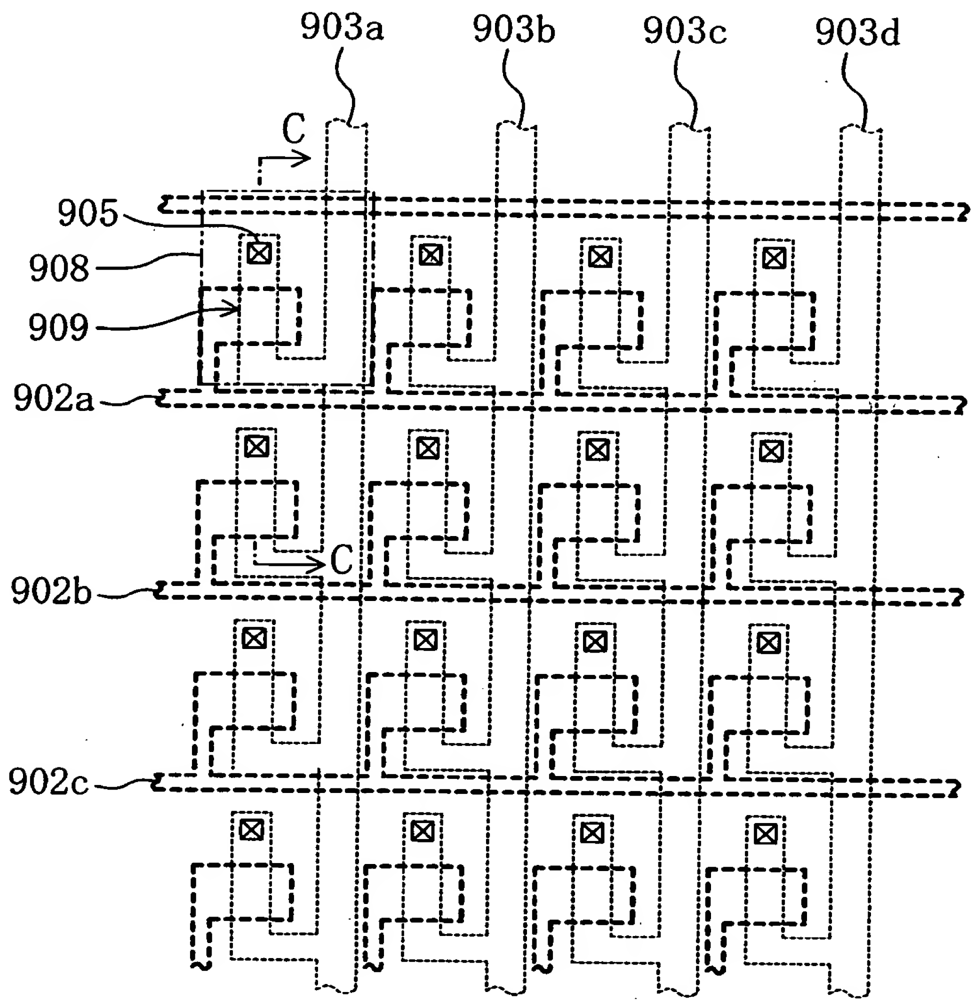

808a
808b
805a
809a
802a
805b
806a
802b
810
809b
807a
807b
802c
806b
802d

【図２２】

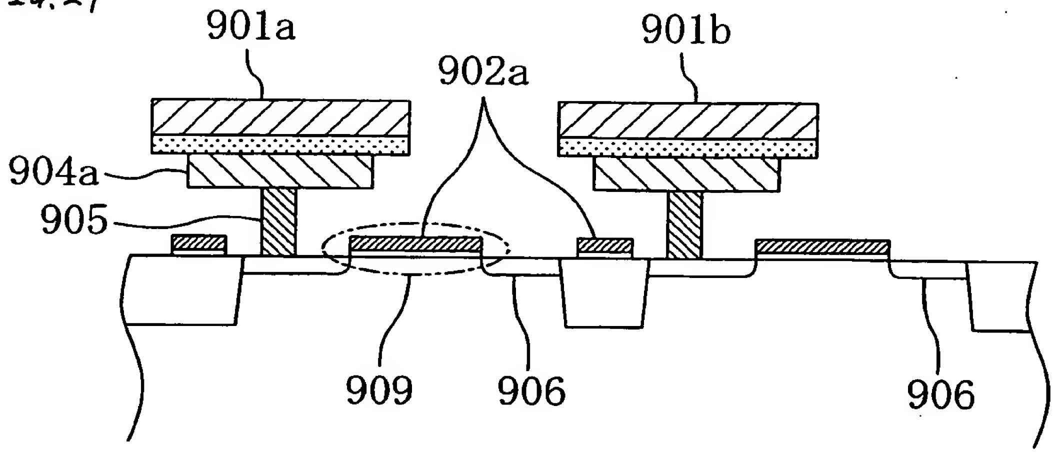
FIG. 22


903a
903b
903c
903d
904a
904b
904c
904d
C
C
905
901a
908
909
902a
901b
902b
901c
902c
901d
b1
c1

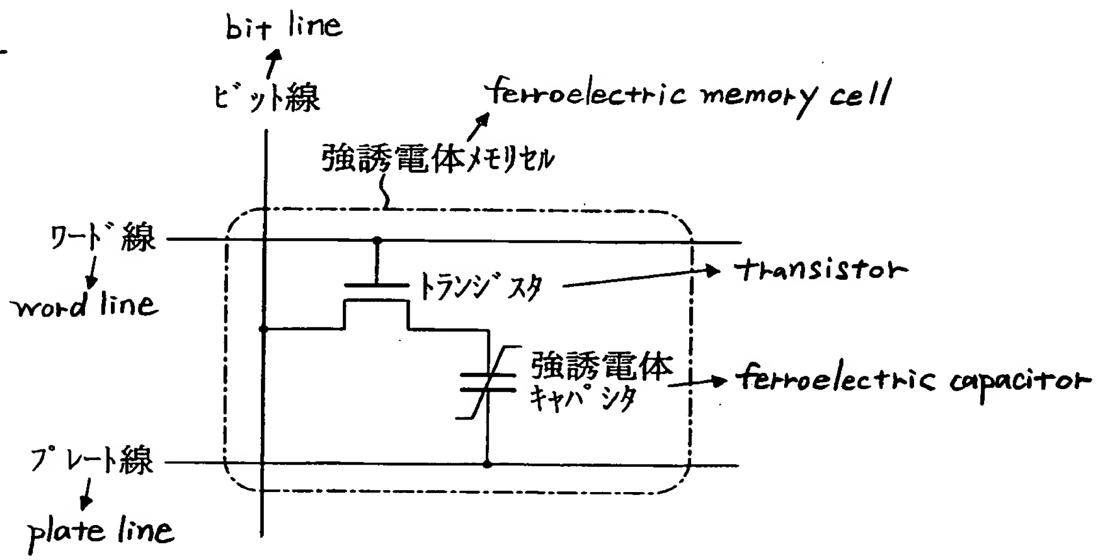
【図２３】
FIG.23



【図２４】
↓
FIG. 24

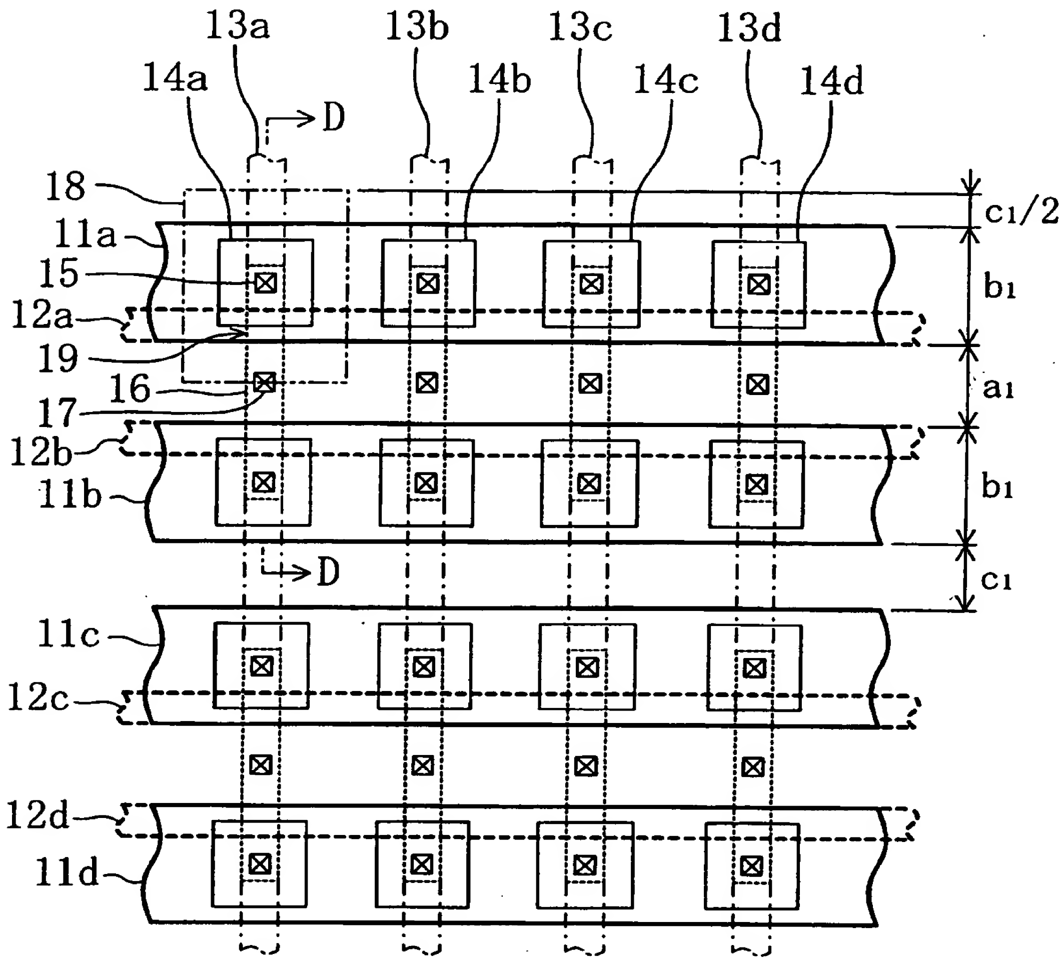


【図２５】
↓
FIG. 25



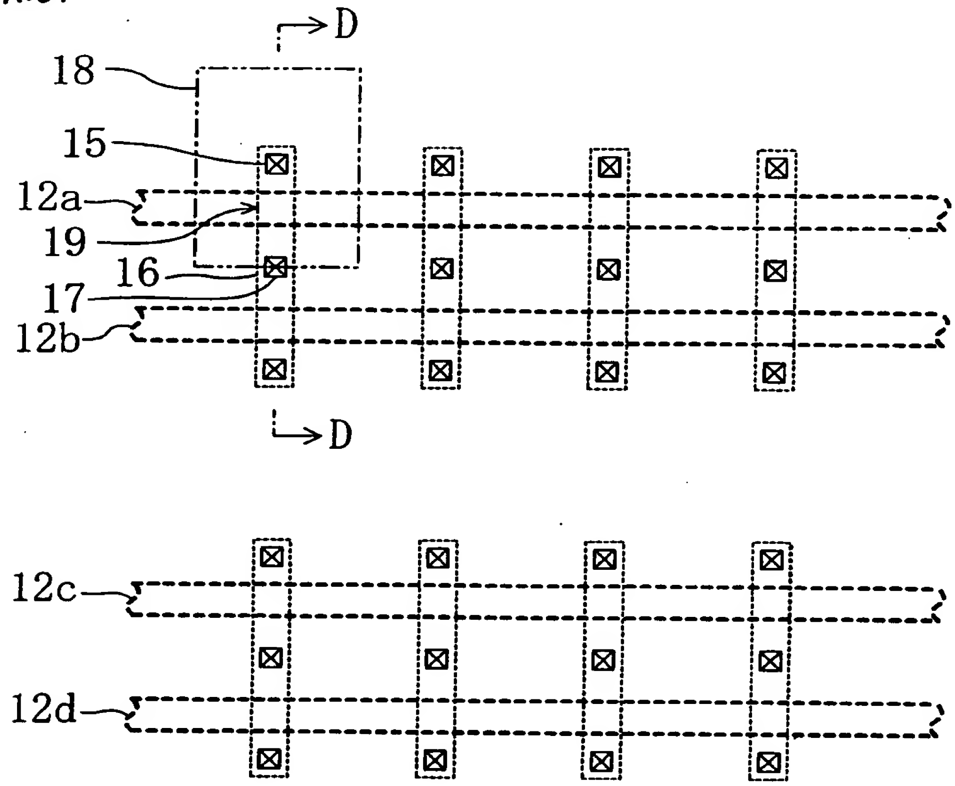
【図２６】

FIG.26


13a
13b
13c
13d
14a
14b
14c
14d
D
18
11a
15
12a
19
16
17
12b
11b
D
11c
12c
12d
11d
c1/2
b1
a1
b1
c1

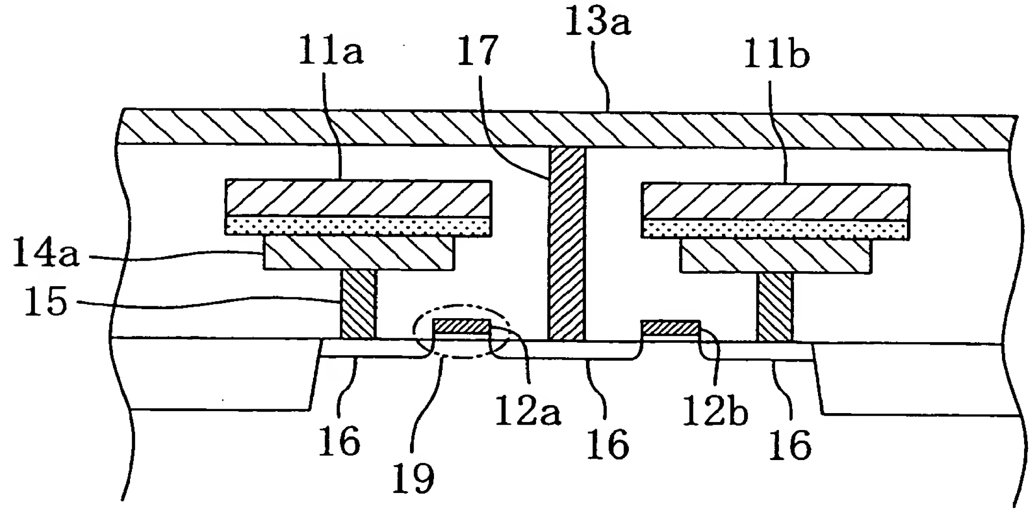
【図２７】

FIG.27



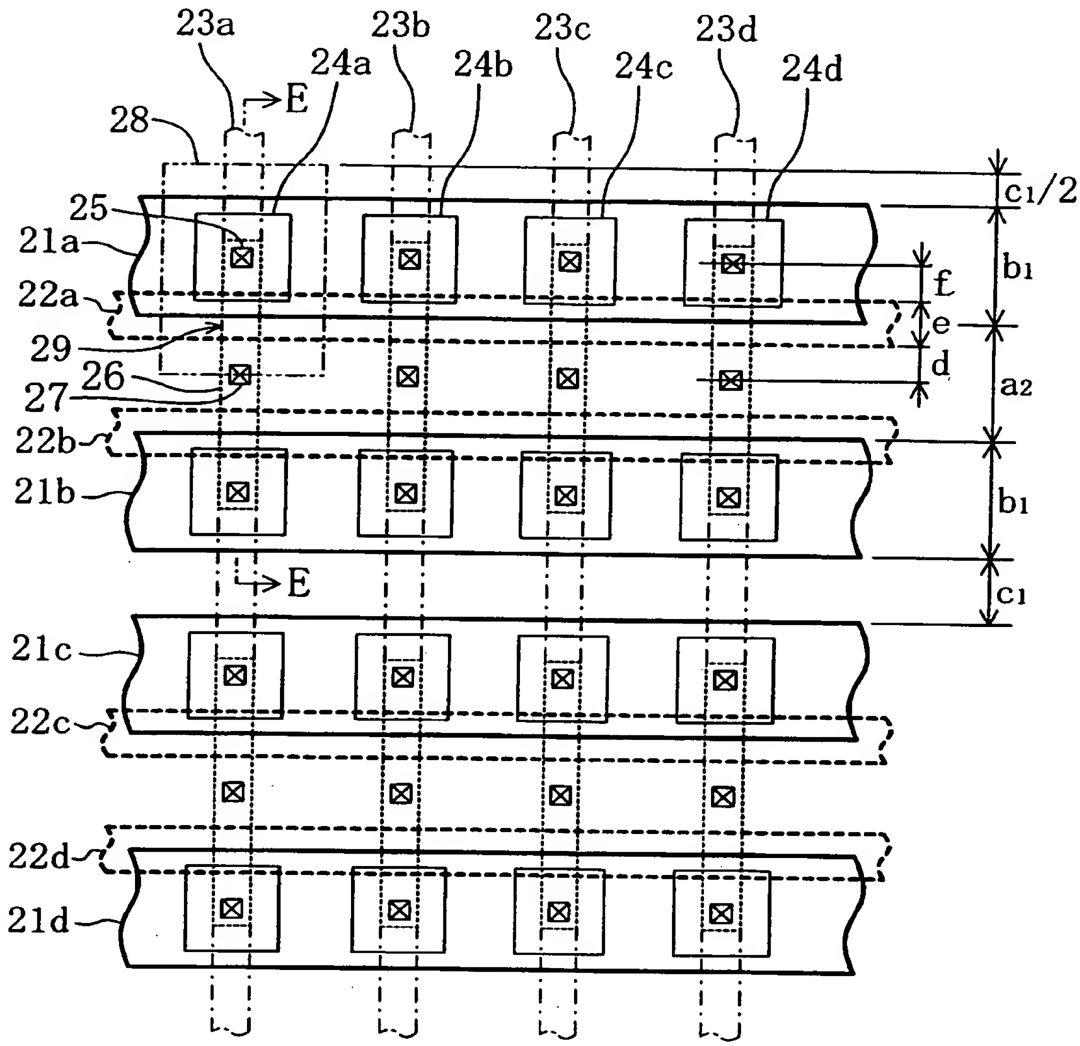
【図２８】

FIG.28



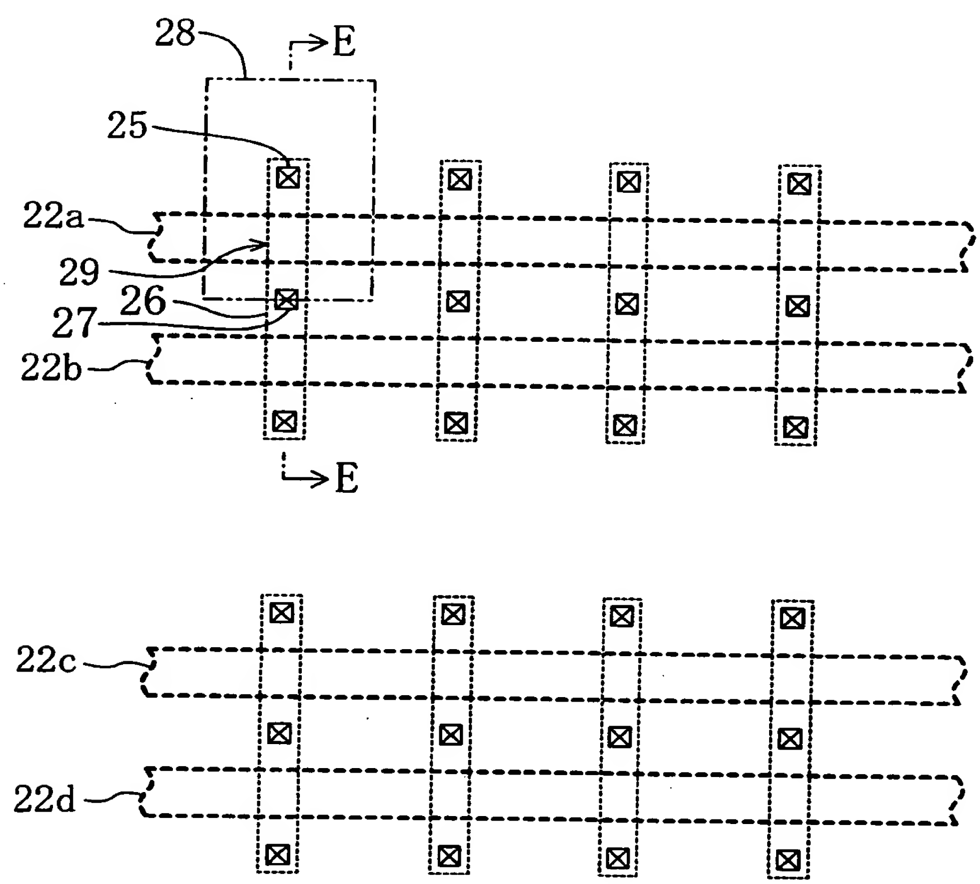
【図２９】

FIG. 29


23a
23b
23c
23d
24a
24b
24c
24d
28
E
25
21a
22a
29
26
27
22b
21b
21c
22c
22d
21d
$c_1/2$
b_1
f
e
d
a_2
b_1
c_1

【図３０】

FIG. 30



【図３１】

FIG. 31